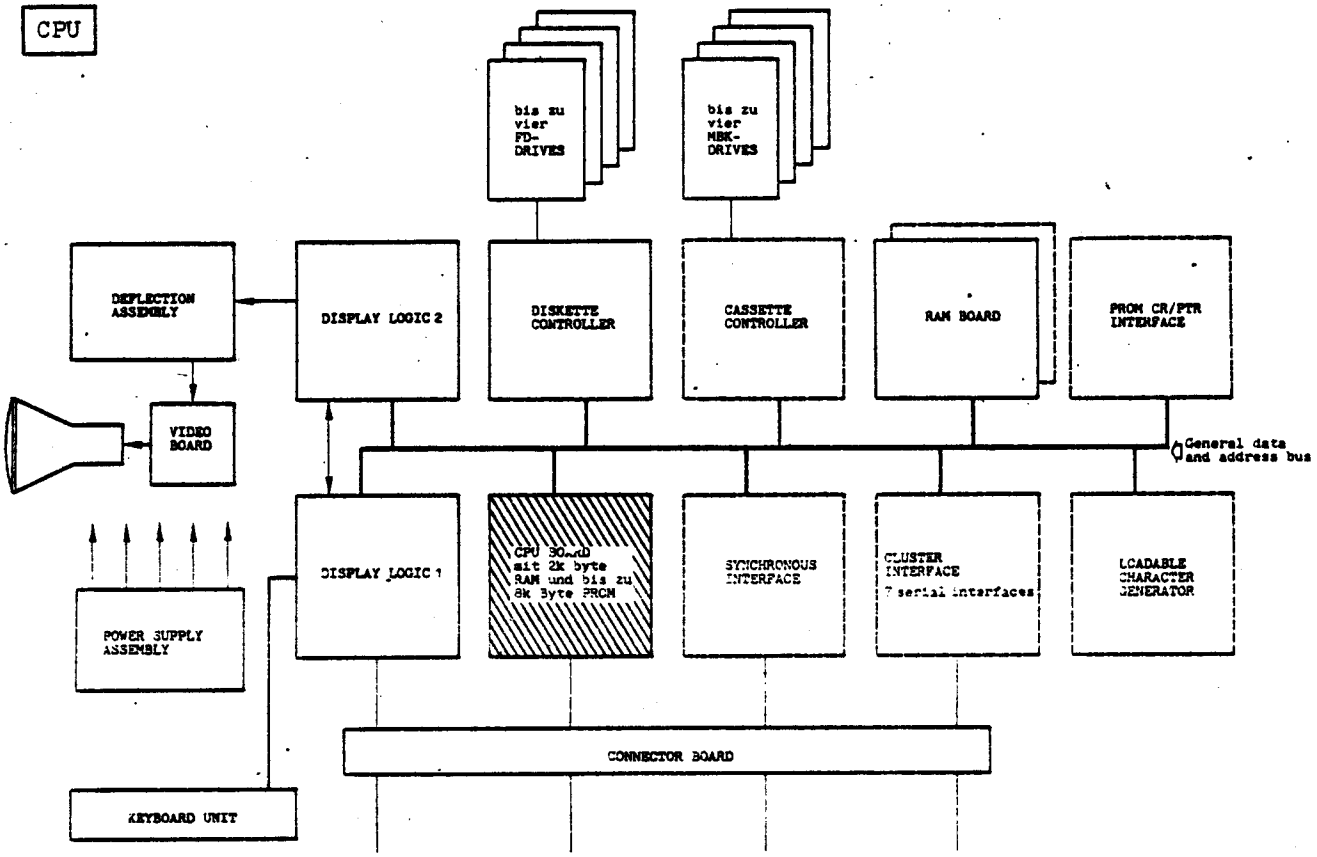
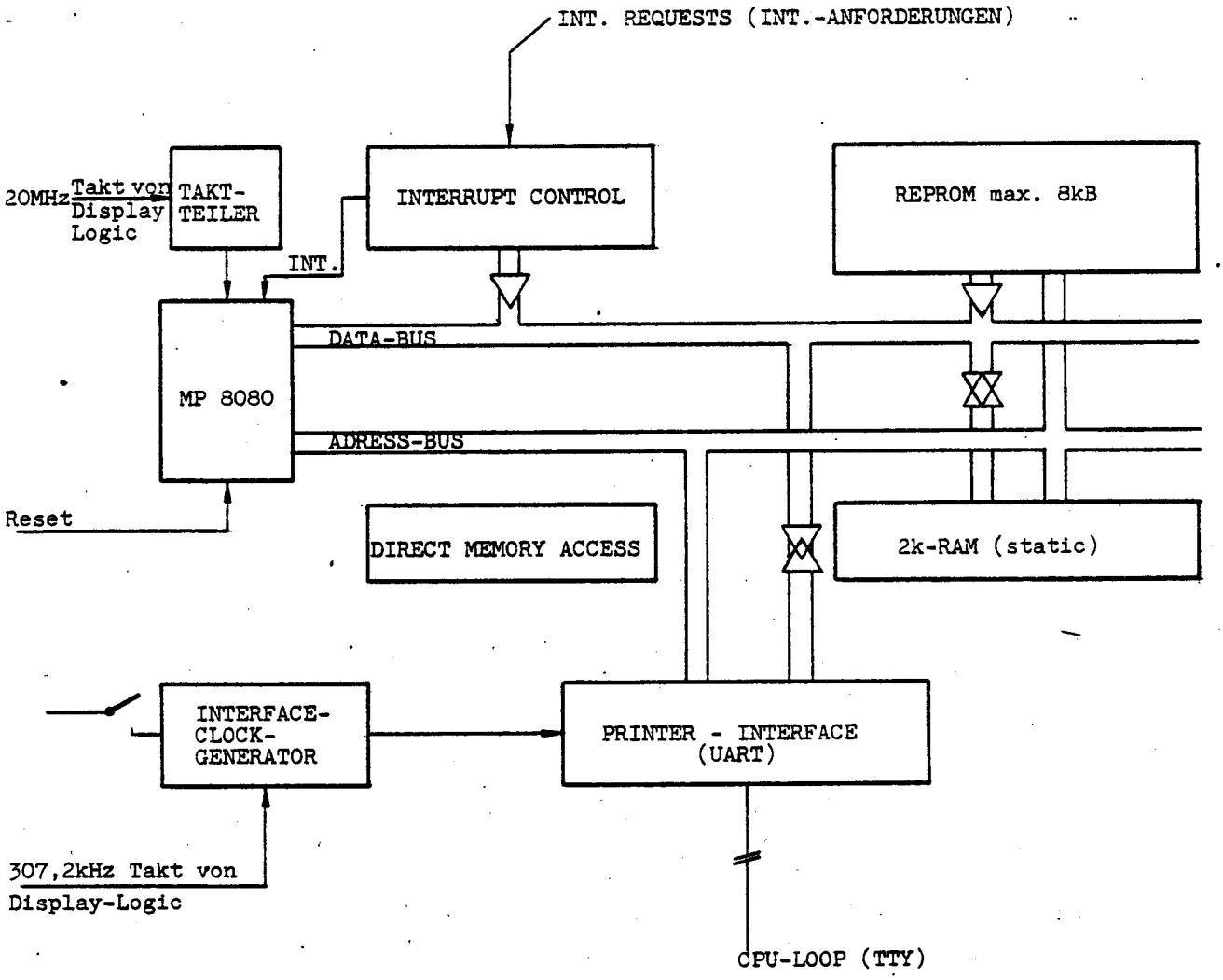


BLOCKSCHALTBILD



MC 80.80

Kern der CPU-Baugruppe ist der Micro-Prozessor 80 80. Er steuert sämtliche Aktivitäten des Gerätes. Ein Takt (20MHz) versorgt den MP80 80 mit den erforderlichen Maschinentakten ϕ1 und ϕ2. Über eine Reset-Leitung wird der MP veranlaßt ab Speicheradresse 0000H mit der Befehlsausführung zu starten. Die Reset-Funktion kann angestoßen werden:

- -durch die Stromversorgung beim Einschalten oder nach Fehler
- -vom Bediener durch Drücken der Reset-Taste.

INTERUPT CONTROL

Diese Interuptsteuerung koordiniert bis zu 7 Unterbrechungsanforderungen von peripheren Geräten. (IREQ 1 - 7). Beim Eintreffen einer Anforderung (z.B. Floppy Disk- Controller=IREQ 6) wird ein INT-Signal erzeugt, das dem MP 80 80 veranlaßt die INT-Anforderung zu untersuchen und in entsprechende Programmroutinen zu verzweigen. (RESTART)

DIRECT MEMORY ACCESS

Diese Steuerung übernimmt die Koordination des Datenverkehrs zwischen den schnellen peripheren Geräten (Floppy, Cassette) und dem gemeinsamen RAM.

REPROM

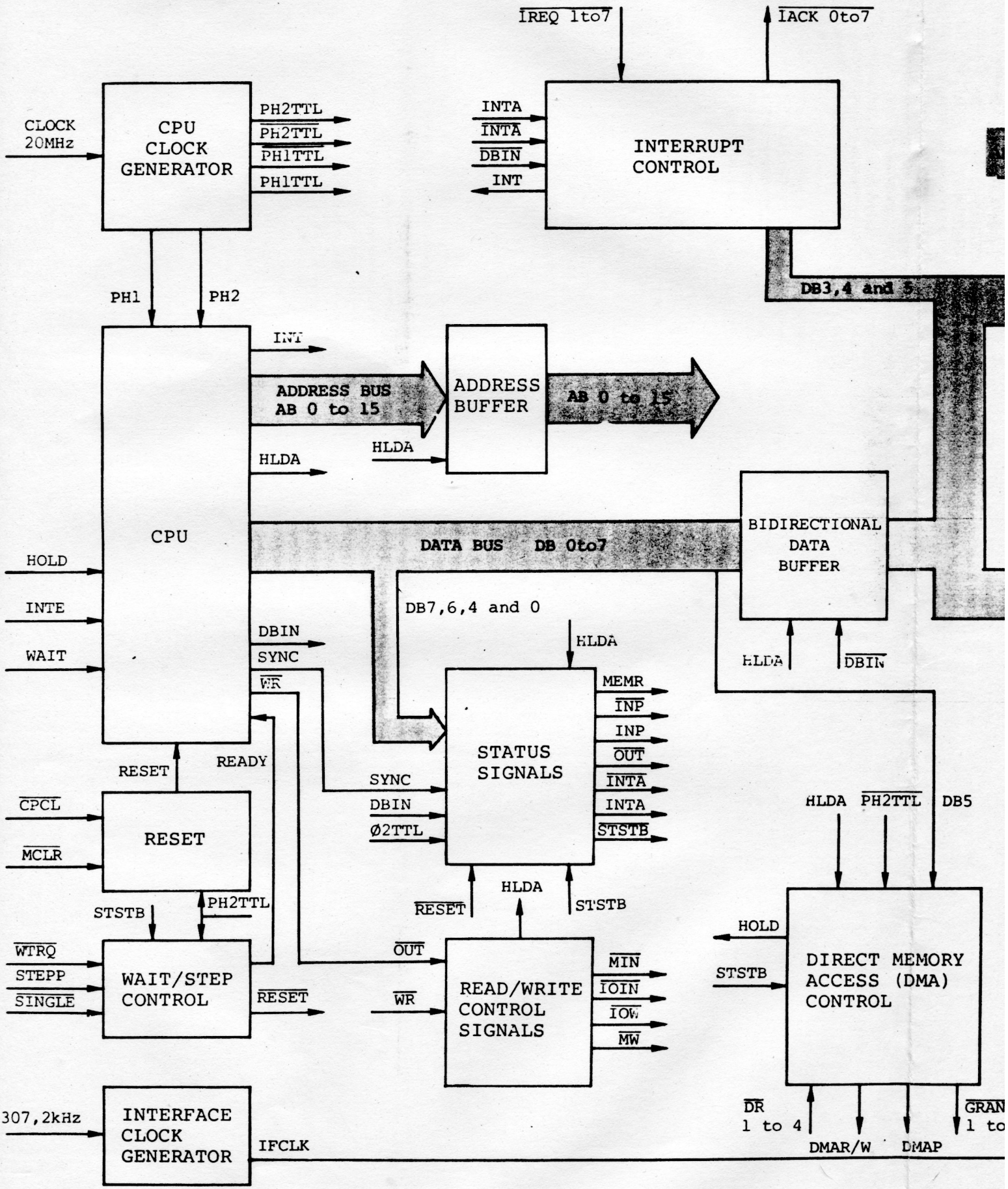
Festprogrammierter Speicher ausbaubar bis max. 8kB. Beinhaltet UR-Lade-Routinen, physikalische E/A-Routinen sowie einige Testhilfen. Die Firmware die der REPROM enthält wird MONITOR genannt.

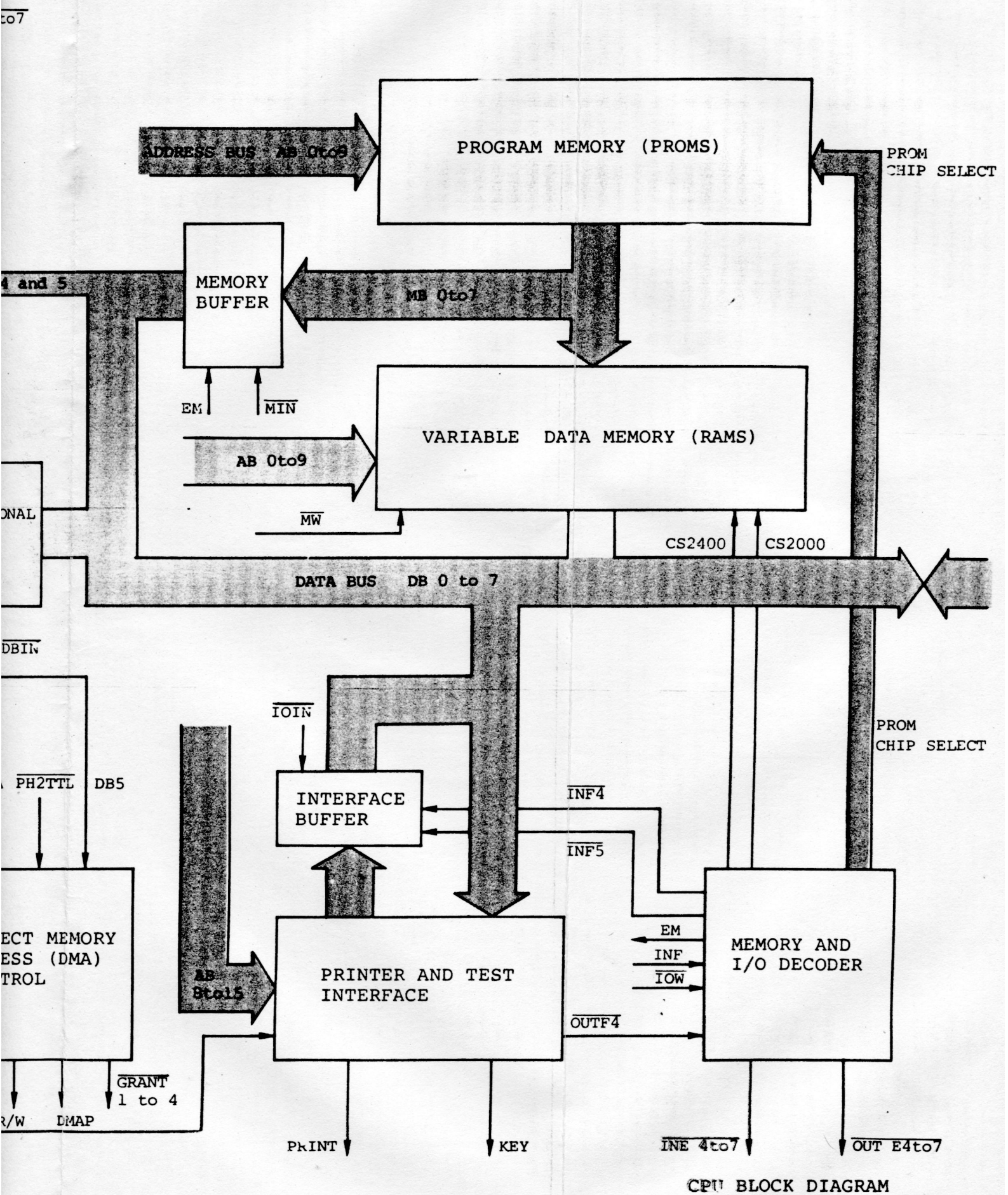
RAM

Statischer Speicher der vom Betriebssystem u.a. als STACK genutzt wird.

PRINTER INTERFACE ≙ CPU-LOOP

Anschlußsteuerung eines Peripheren Gerätes mit TTY-Current Loop-Schnittstelle (Drucker). Ein UART-Baustein übernimmt die Sende/Empfangssteuerung, sowie die Paritygenerierung und -Prüfung. Ein INTERFACE CLOCK GENERATOR versorgt den UART-Baustein mit dem erforderlichen Datenübertragungstakt. Der Service-Techniker hat die Möglichkeit diesen Takt einzustellen. (75 bis 9600 b/s)
Weitere Einstellmöglichkeiten:
Parity-Prüfung und Wortlänge.


IREQ 1to7
IACK 0to7
CLOCK 20MHz
CPU CLOCK GENERATOR
PH2TTL
PH2TTL
PH1TTL
PH1TTL
INTA
INTA
DBIN
INT
INTERRUPT CONTROL
DB3,4 and 5
PH1
PH2
INT
ADDRESS BUS AB 0 to 15
ADDRESS BUFFER
AB 0 to 15
HLDA
HLDA
CPU
DATA BUS DB 0to7
BIDIRECTIONAL DATA BUFFER
HOLD
INTE
WAIT
DB7,6,4 and 0
HLDA
HLDA
DBIN
DBIN
SYNC
WR
MEMR
INP
INP
OUT
INTA
INTA
STSTB
STATUS SIGNALS
SYNC
DBIN
Ø2TTL
RESET
READY
HLDA PH2TTL DB5
CPCL
MCLR
RESET
RESET
HLDA
STSTB
STSTB
PH2TTL
HOLD
STSTB
DIRECT MEMORY ACCESS (DMA) CONTROL
WTRQ
STEPP
SINGLE
WAIT/STEP CONTROL
RESET
OUT
WR
READ/WRITE CONTROL SIGNALS
MIN
IOIN
IOW
MW
DR 1 to 4
DMAR/W
DMAP
GRAN 1 to
307,2kHz
INTERFACE CLOCK GENERATOR
IFCLK



CPU BLOCK DIAGRAM

CPU CLOCK GENERATOR

The CPU is working with a clock period of 0.4932 µs which equals 2.02752 MHz. This is obtained by dividing a 20.2752 MHz frequency by 10. The 20.2752 MHz crystal oscillator is located on the Display Logic board. The dividing is done in the counter U46 coupled to divide by 10.

The divide by 5 output, pin 2, and the divide by 10 output, pin 5, are gated by U51 to form PH1TTL. See timing diagram page 00.

PH1TTL and PH2TTL are coupled to the high level MOS driver U45 via C1 and C2. CR1 keeps pin 3 at − 0.7 volts to ensure that PH1 and PH2 really are at ground level when low. See also pages 3-2 and 3-3 in the INTEL 8080 manual.

CPU

See the INTEL 8080 manual for a detailed description of the microprocessor.

ADDRESS BUFFER

The Address Buffer acts as driver for the encoded addresses that the CPU enter onto the address bus. When HLDA is true, the two 8 Bit Address Buffers are in the tri-state and the CPU is separated from the address bus.

See also page 3-5 in the INTEL 8080 Manual.

INTERRUPT CONTROL

The interrupt system consists of one priority encoder, one D-type reg outputs, and one decoder.

There are seven Interrupt Request lines ranked after decreasing priori the highest priority, IREQ7 the lowest.

An Interrupt Request appearing on any of the IREQ inputs will cause be fed from the priority encoder U49 to the CPU, U31 and the enco the register U44. When the CPU ackonwledges the interrupt, a RES corresponding to the active request line with the highest priority is fe true and clocks the encoded Interrupt Request onto the data bus when The encoded Interrupt Request is simultaneously fed into the decoder as an Interrupt Acknowledge, IACK to the device th interrupt in the first place.
The interrupt system is enabled by the instruction E1, an instruction D1.

Level	Device	Restart Address
0	RESET (Overriding)	0
1	DISPLAY REFRESH LOGIC	8 (50 times/sec
2	SYNC. INTERFACE	10 (HEX)
3	MASTER DISPLAY	18 (HEX)
4	CLUSTER INTERFACE	20 (HEX)
5	SPARE (CLUSTER INTF. II)	28 (HEX)
6	FLOPPY DISK CONTROL	30 (HEX)
7	CASSETTE CONTROL	38 (HEX)

See also page 2-11 in the INTEL 8080 manual.

BIDIRECTIONAL DATA BUFFER

The Bidirectional Data Buffer consists of two 8 Bit Input/Output Ports governed by the DBIN and the HLDA signals. When DBIN goes true U27 will connect the data bus to the CPU while U28 will be in its tri-state. When DBIN goes false U28 which points away from the CPU will allow data onto the data bus while U27 is in its tri-state mode.

When HLDA goes true both ports are in their tri-state and the external device which requested the HOLD take control of the busses. Both ports acts as drivers when not in their tri-state.

RESET

The CPU can be reset either by the CPUCL signal from a pushbutton on the front of the display unit or by the MCLR signal from the Power Supply. Either one of these signals will make the D input of the flip-flop go high, and the next positive going edge of the PH2TTL pulse will make the RESET signal go true. A reset will make the program counter start running from zero, addressing the monitor program.

WAIT/STEP CONTROL

If the variable data memory on the RAM board wants the CPU to wait, e.g. during a refresh period, XWTRQ goes true. This will indicate that no stable data is available on the data bus. WTRQ true will cause the D input of U58 to go low and the READY output, pin 9 will go false on the next positive goind edge of PH2TTL. This will bring the CPU into a wait period.

For test purposes, provisions are made on the CPU board for manually stepping the CPU through a program. First the SINGLE line must be held low, and then a bouncefree pulse must be applied to the STEP input. Evere pulse will cause the CPU to proceed one cycle.

See page 2-5 in the INTEL 8080 manual.

STATUS LATCH

Four of the eight data bus lines are used to generate the status signals MEMR, INP, OUT, and INTA, U55 being clocked by the status strobe STSTB. MEMR designates that the data bus will be used for memory read data. INP indicates that the address bus contains the address of an input device and that input data from this device should be placed on the data bus when DBIN is true. OUT indicates that the address bus contains the address of an output device and the data bus will contain the output data when WR is active. INTA is the acknowledge signal for interrupt request.

The status strobe STSTB is formed by AND-ing the SYNC signal from the CPU with the PH2TTL signal.

The tri-state drivers on the status lines can be disabled by the HLDA signal.

The status latch will store the CPU status information during the whole information cycle.

See pages 2-6 and 3-5 in the INTEL 8080 manual.

DMA CONTROL

The Direct Memory Access systems memory from up pointers and word counters

The DMA Control monitors ber, the higher the priority. L fetch cycle only, and GRA the appropriate GRANT li exeption is DMA channel 1 active. In addition to the G carry the information the G

The DMA-channels are alloca

DMA-channel	Device
1 (DR1)	Test
2 (DR2)	Floppy
3 (DR3)	Cassette
4 (DR4)	(Spare)

When, for example, DR2 go ster U41 goes high. Pin 5 als when the STSTB goes high a When the CPU acknowledges tive going edge of PH2TTL goes true.

On the next positive going ed to go true. On the negative enabled and DMAPLS goes tr

On the fourth PH2TTL pulse 1750 us. See the timing diagr

INTERFACE CLOCK GENERATOR

The Printer and Test Interface may operate at different speeds, selectable with a switch arrangement on the CPU board.

9600, 4800, 2400, 1200, 600, 300, and 75/110 baud can be obtained by closing the switch representing the desired speed. The 75/100 baud switch gives 110 baud if the "110 Baud Disable" switch is open.

The 307.2 kHz signal from the Display Logic clocks two counters which divide by 2, 4, 8, 16, 64, and 256, respectively. The selected frequency is fed to the UART U30 of the Printer and Test Interface. The UART requires the clockpulse to be 16 times that of the transfer rate so that for example a transfer rate of 9600 baud requires an IFCLK frequency of 153.6 kHz, i.e. 307.2 kHz divided by two.

READ WRITE CONTROL SIGNALS

The control signals MIN, IOIN, IOW, and MW are generated by gating the DBIN and WR signals from the CPU with the status signals MEMR, INP, and OUT.

All four control signal lines are buffered by U60 which will keep the lines floating when HLDA is true.

See page 3-5 in the INTEL 8080 manual.

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There are seven Interrupt Request lines ranked after decreasing priority, i.e. IREQ1 has the highest priority, IREQ7 the lowest.

An Interrupt Request appearing on any of the IREQ inputs will cause the INT signal to be fed from the priority encoder U49 to the CPU, U31 and the encoded signal to enter the register U44. When the CPU ackonwledges the interrupt, a RESTART instruction corresponding to the active request line with the highest priority is fetched. INTA goes true and clocks the encoded Interrupt Request onto the data bus when it is unoccupied. The encoded Interrupt Request is simultaneously fed into the decoder U43 and returned as an Interrupt Acknowledge, IACK to the device that requested the interrupt in the first place.
The interrupt system is enabled by the instruction E1, and disabled by the instruction D1.

Level	Device	Restart Address
0	RESET (Overriding)	0
1	DISPLAY REFRESH LOGIC	8 (50 times/sec.)
2	SYNC. INTERFACE	10 (HEX)
3	MASTER DISPLAY	18 (HEX)
4	CLUSTER INTERFACE	20 (HEX)
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MEMORY BUFFER

The Memory Buffer acts as a switch and a driver on the data bus to the Program Memory (PROM) on the CPU board. If either the Memory Input, MIN, or Enable Memory, EM signals or both are false, the Memory Buffer enters its tri-state mode and disconnects the Program Memory from the data bus. If MIN and EM both are true, it acts as a driver.

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The Bidirectional Data Buffer consists of two 8 Bit Input/Output Ports governed by the DBIN and the HLDA signals. When DBIN goes true U27 will connect the data bus to the CPU while U28 will be in its tri-state. When DBIN goes false U28 which points away from the CPU will allow data onto the data bus while U27 is in its tri-state mode.

When HLDA goes true both ports are in their tri-state and the external device which requested the HOLD take control of the busses. Both ports acts as drivers when not in their tri-state.

STATUS LATCH

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The status latch will store the CPU status information during the whole information cycle.

See pages 2-6 and 3-5 in the INTEL 8080 manual.

DMA CONTROL

The Direct Memory Access Control circuit can control the data transfer to and from the systems memory from up to four devices connected to the general data bus. Address pointers and word counters must be located on the devices.

The DMA Control monitors four DMA Request lines, DR1 to DR4. The lower the number, the higher the priority. Line 1 is overriding. DMA transfer can take place in a memory fetch cycle only, and GRANT is not given before the CPU has read its instruction. Then the appropriate GRANT line becomes active, and remains so for one microsecond. An exeption is DMA channel 1, where GRANT will remain active as long as the request is active. In addition to the GRANT line to each device, a signal DMA R/W is activated, to carry the information the GRANT has been given.

The DMA-channels are allocated as follows:

DMA-channel	Device
1 (DR1)	Test
2 (DR2)	Floppy Disc Controller
3 (DR3)	Cassette Controller
4 (DR4)	(Spare)

When, for example, DR2 goes true, the corresponding output, pin 9 on the priority register U41 goes high. Pin 5 also goes high and on the CPUs next FETCH cycle DB5 is high when the STSTB goes high and consequently clocks U47 and thus makes HOLD go true. When the CPU acknowledges the HOLD request, HLDA goes true and on the next positive going edge of PH2TTL pin 9 on U47 goes high. This enables U42 and GRANT 2 goes true.

On the next positive going edge of PH2TTL pin 5 on U48 goes high and causes the DMARW to go true. On the negative going edge of the same PH2TTL the decoder (LS 139) is enabled and DMAPLS goes true.

On the fourth PH2TTL pulse GRANT is turned off after having been on for maximum 1750 us. See the timing diagram on page 00.

READ WRITE CONTROL SIGNALS

The control signals MIN, IOIN, IOW, and MW are generated by gating the DBIN and WR signals from the CPU with the status signals MEMR, INP, and OUT.

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See page 3-5 in the INTEL 8080 manual.

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IC. INTERFACE	10 (HEX)
STER DISPLAY	18 (HEX)
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RE (CLUSTER INTF. II)	28 (HEX)
PPY DISK CONTROL	30 (HEX)
SETTE CONTROL	38 (HEX)

2-11 in the INTEL 8080 manual.

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MEMORY AND I/O DECODER

The CPU must be able to communicate with devices such as for example keyboards, displays, printers, and diskette drives that exist outside its normal memory array. With its 16 bit address bus the CPU is able to address up to 64 k of RAM or PROM memory.

The CPU places the memory address code or the port address code of the device it wishes to communicate with on the address bus. This code is decoded by U35 and U36 which are governed by the status signal INP and the control signal IOW to activate the proper output or input line. The outputs of U37 are gated by U39 to give the Enable Memory signal EM which enables the memories on the CPU board. The two chip select signals used by the static RAM on the CPU board are also generated by U37.

U38 generates the eight chip select signals to the PROM located on the CPU board.

See also page 3-8 in the INTEL 8080 manual.

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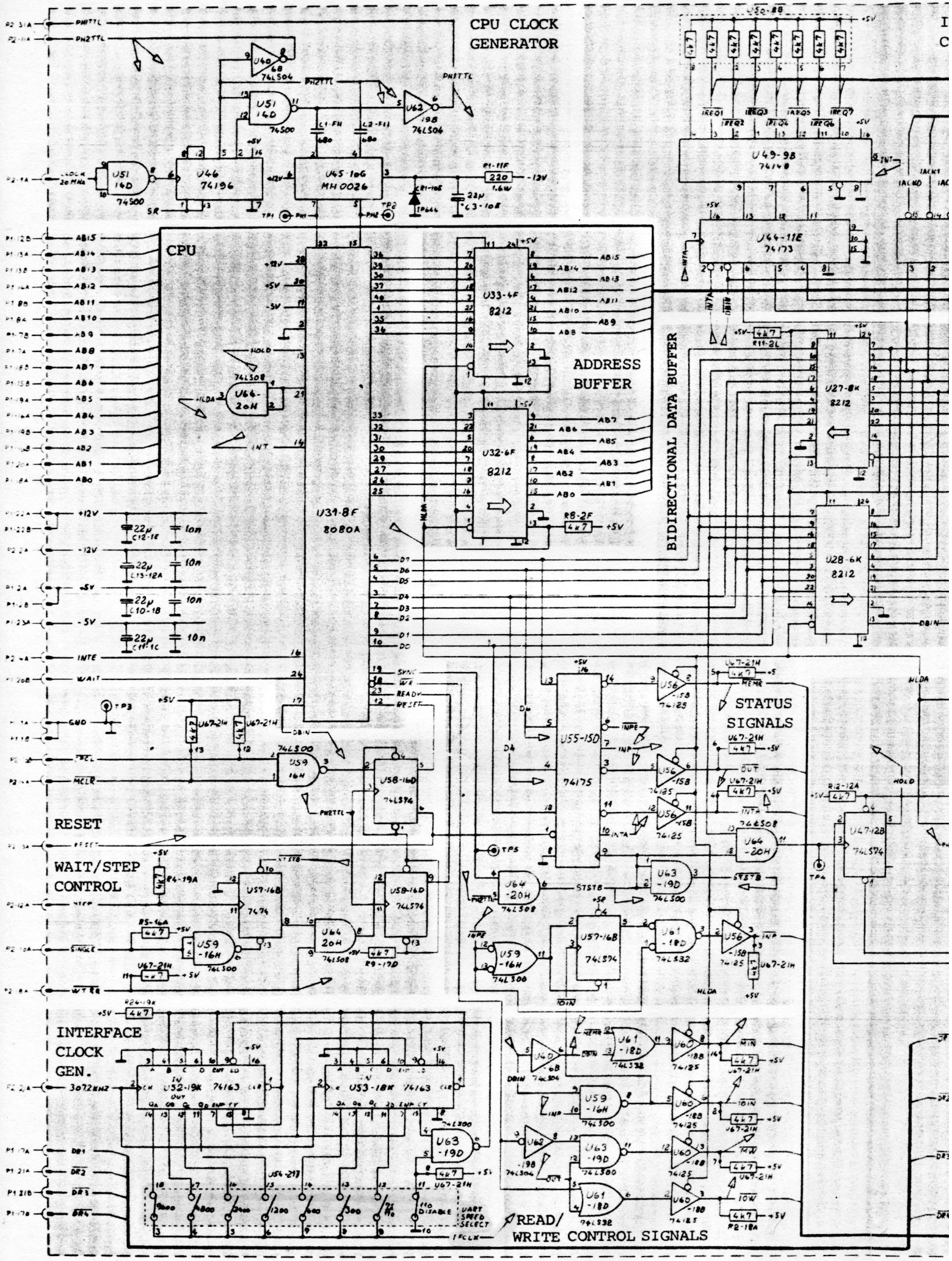
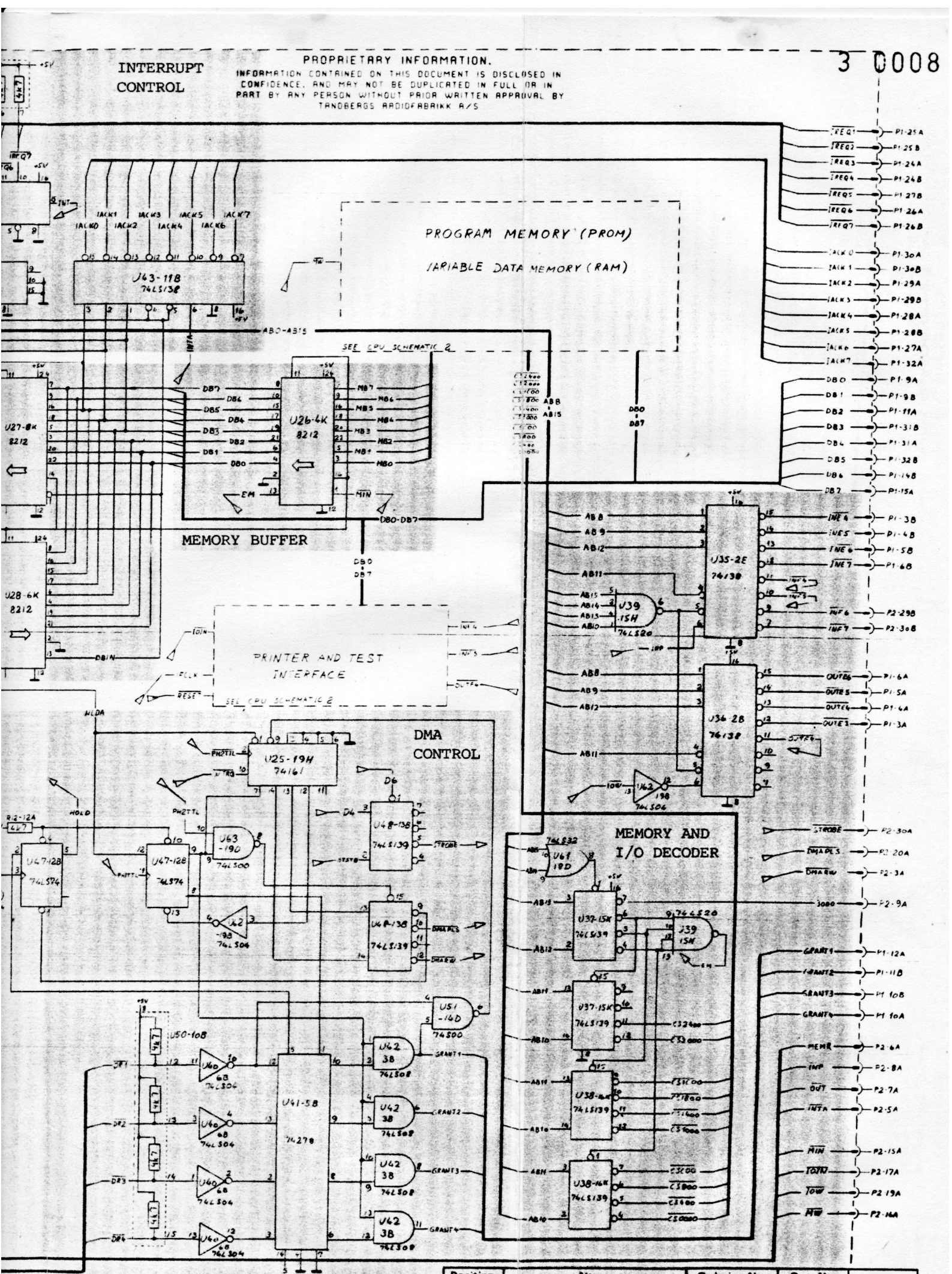

CPU CLOCK GENERATOR
CPU
ADDRESS BUFFER
BIDIRECTIONAL DATA BUFFER
STATUS SIGNALS
RESET
WAIT/STEP CONTROL
INTERFACE CLOCK GEN.
READ/ WRITE CONTROL SIGNALS
U49-9B 74148
U44-11E 74173
U33-4F 8212
U32-6F 8212
U31-8F 8080A
U27-8K 8212
U28-6K 8212
U55-15D 74175
3072KHZ
UART SPEED SELECT

INTERRUPT CONTROL



Position	Name	Ordering No.	Rev. No.	Date
A5	CPU (Schematic 1)	960313	010	28.2.77

PROGRAM MEMORY (PROM)

The activity of the CPU is directed by a program which consists of a series of logically related instructions. These instructions are stored in the Program Memory. Sockets are provided for up to eight 1024x8 bit Erasable and Electronically Reprogrammable Read Only Memory packages, called PROMS, which may be taken out, erased and reprogrammed. The eight PROMS are connected to the data bus through the Memory Buffer.

Each instruction has its own address and the CPU will ask for instructions in sequence by placing an address on the address bus. These addresses go directly to each of the PROMS. They are also decoded in the Memory and I/O Decoder to generate the Chip Select, CS, signals for the PROMS.

See also pages 1-1 and 3-6 in the INTEL 8080 manual.

VARIABLE DATA MEMORY (RAM)

The variable data memory can store program data, active "look-up tables" and temporary values (or external stacks). The variable data memory is different from the program memory bacause data can be both written into it and read out of it.
Each RAM is connected to the address bus but eight RAMs share the same chip select, CS, signal because they have only one output each.

See also pages 1-1 and 3-6 in the INTEL 8080 manual.

PRINTER AND TEST INTERFACE

A current loop Printer and Test Interface is supplied for test purposes and the possibility of connecting a hard copy printer to the display unit. Data from an external device enters through R22 and activates the LED in the opto coupler U66 whenever data is low. Consequently data enters the Universal Asynchronous Receiver Transmitter (UART) in series form on pin 20. The UART converts the data into parallel form and transfers it to the tri-state Input/Output Port U29 when the decode address F4 occurs. The UART status word is transferred when F5 is active. U29 acts as a driver and feeds the status or data onto the data bus when IOIN goes true. In this phase the inputs of the UARTs are open. When data on the bus is intended for the printer, U29 is in its tri-state mode and the data on the bus enter directly into the UART. The UART converts the data from parallel to series form and feeds it through the opto coupler U65 onto the printer current loops. The current loops are fed from a floating 24 volts power supply with no connections to ground.

Transfer rate of the UART is determined by the interface Clock Generator.

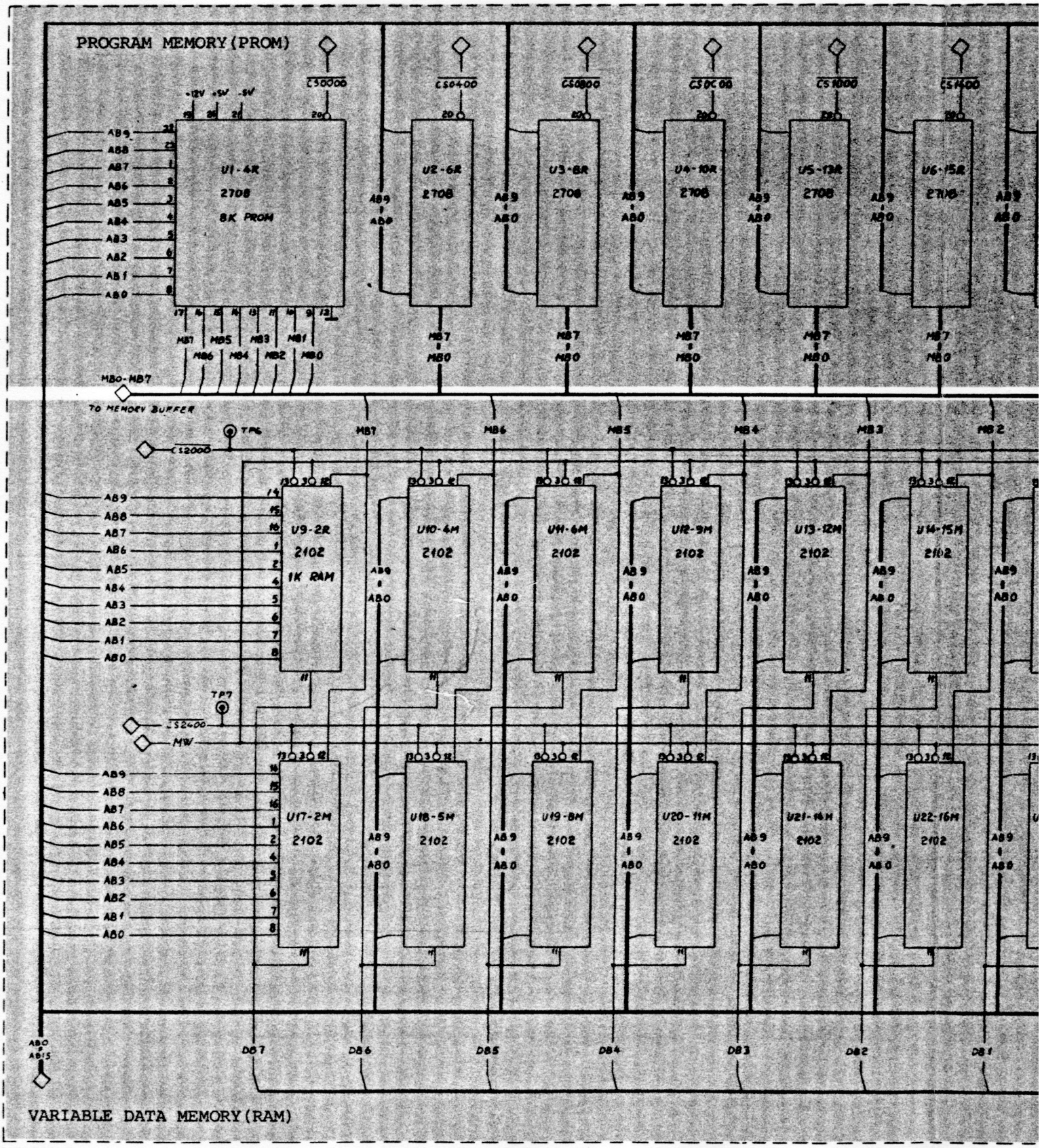
Switch number 1 will select either 7 or 8 bits per character, 7 bits when closed, 8 when open.

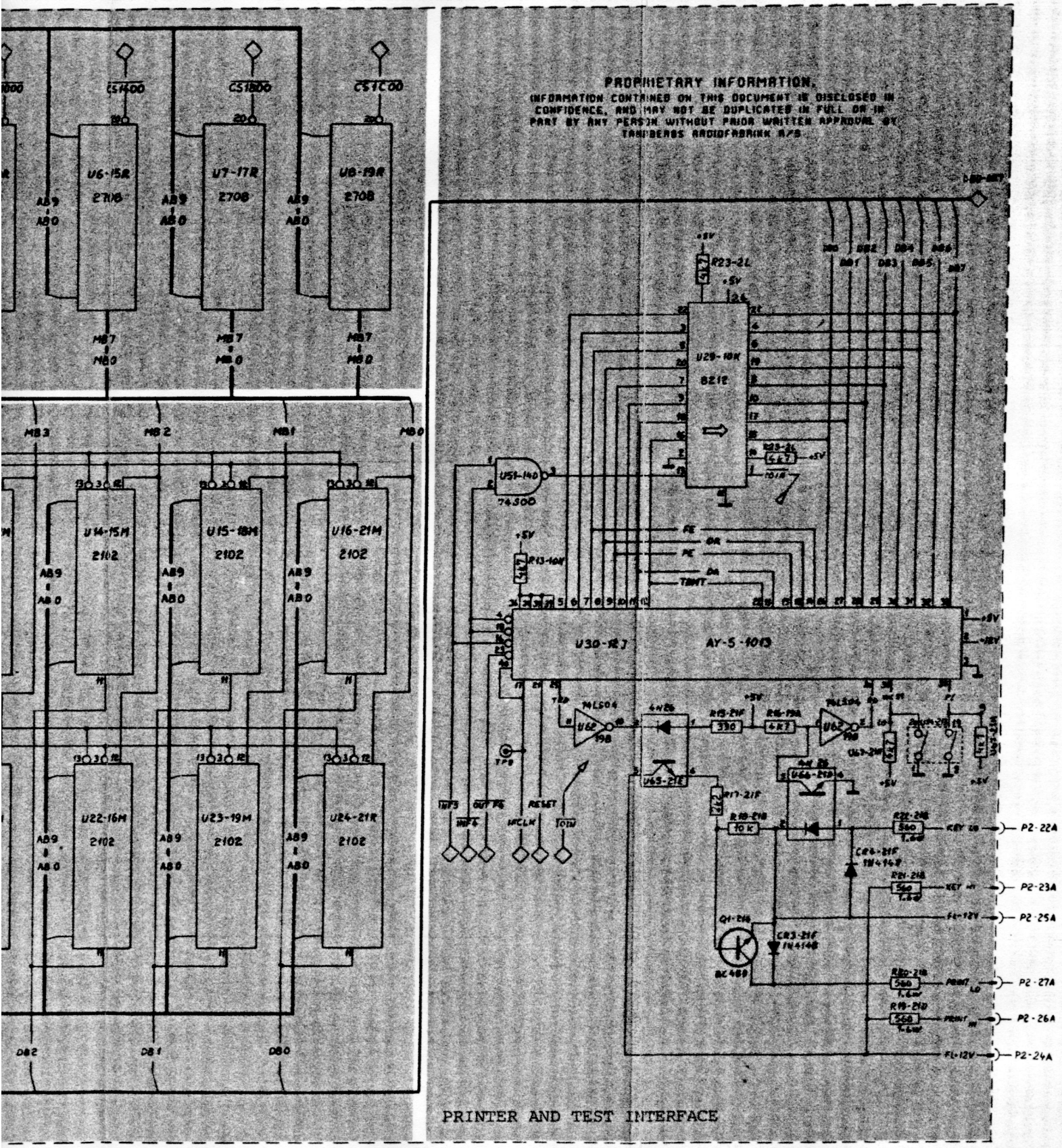
Switch number 2 when open will eliminated the parity bit from the transmitted and received character. Pins 34, 36, 37 and 39 are pulled high through R13. Pin 34 high means that the control bits (EPS, NB1, NB2, TSB, NP) will be entered into the control bits holding register.

Pin 36 select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. Held high, 2 stop bits will be inserted.

Pin 37 high enables switch number 2 to select between 7 and 8 bits per character.

Pin 39 high introduces even parity to be appended immediately after the data bits. It also determines that receiver will check for even parity.


PROGRAM MEMORY (PROM)
U1-4R 2708 8K PROM
U2-6R 2708
U3-8R 2708
U4-10R 2708
U5-13R 2708
U6-15R 2708
MB0-MB7
TO MEMORY BUFFER
U9-2R 2102 1K RAM
U10-4M 2102
U11-6M 2102
U12-9M 2102
U13-12M 2102
U14-15M 2102
U17-2M 2102
U18-5M 2102
U19-8M 2102
U20-11M 2102
U21-14M 2102
U22-16M 2102
VARIABLE DATA MEMORY (RAM)



Position	Name	Ordering No.	Rev. No.	Date
A5	CPU (Schematic 2)	960313	010	28.2.77

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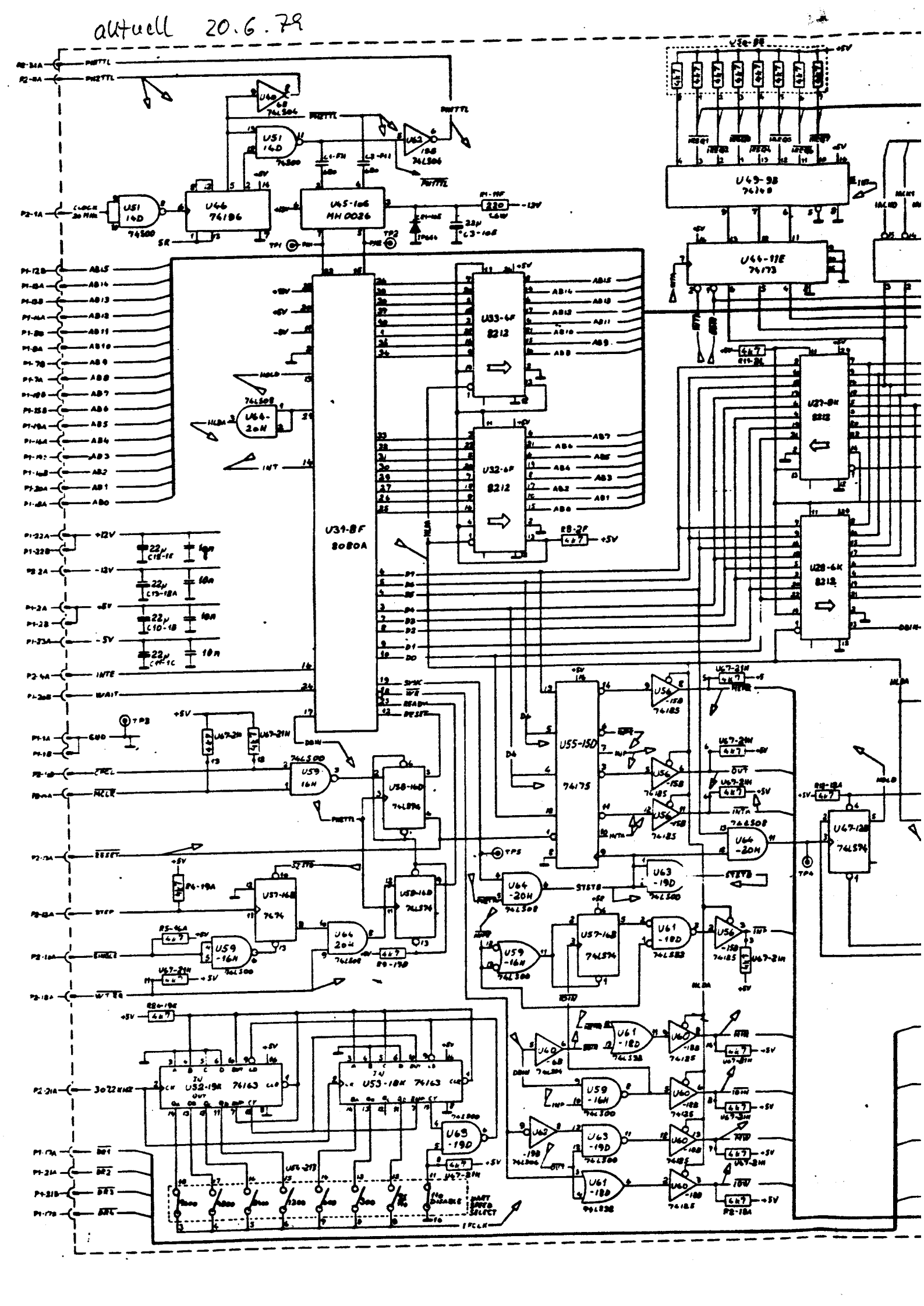

PROGRAM MEMORY (PROM)

VARIABLE DATA MEMORY (RAM)

PRINTER AND TEST INTERFACE

SEE CPU SCHEMATIC 2

U43-11B 74LS138

U26-6K 8212

U23-8H 8212

U28-6K 8212

U35-2E 74LS30

U36-2B 74LS30

U25-19M 74161

U61-5B 74279

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960313 REV 03

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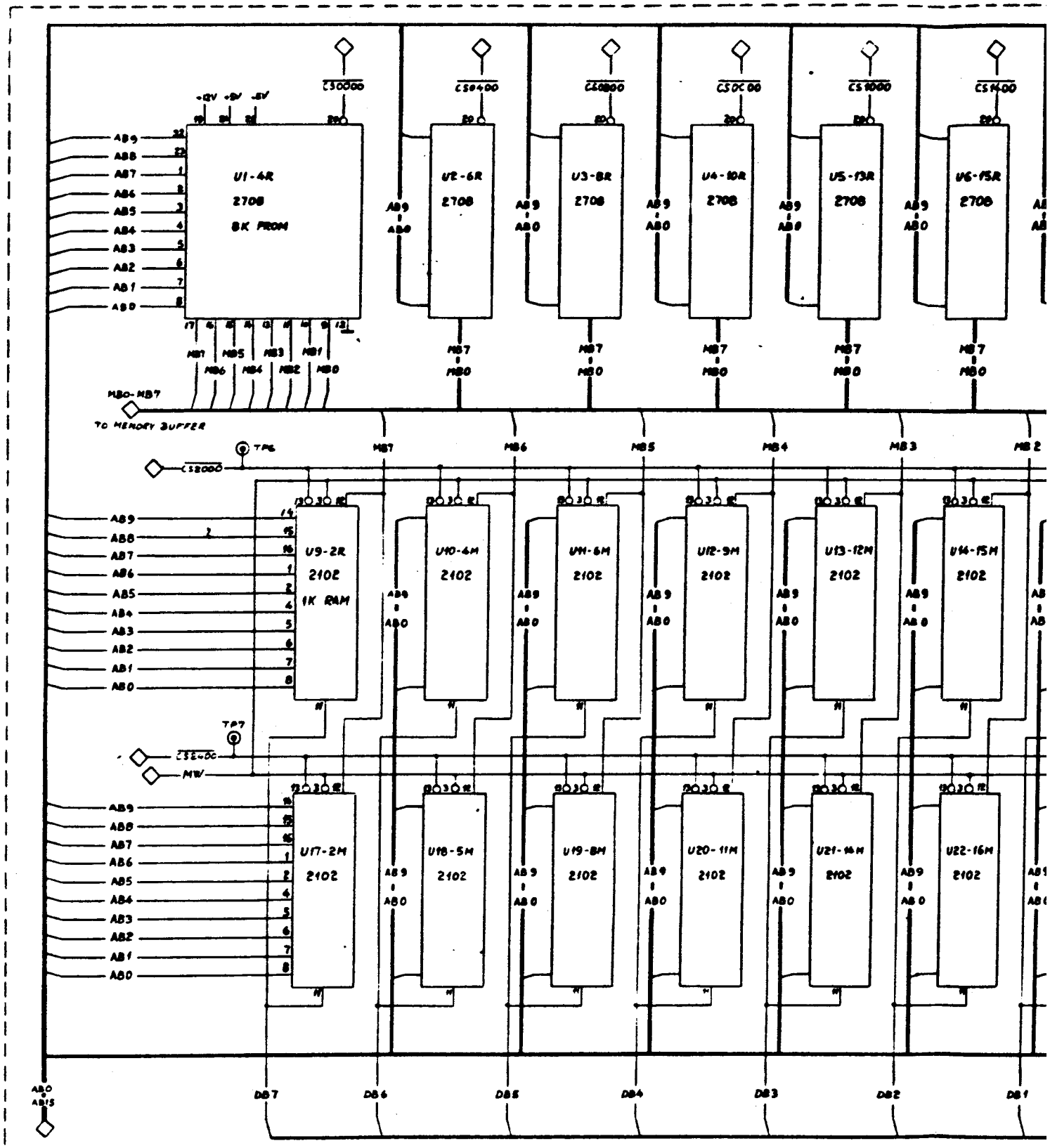

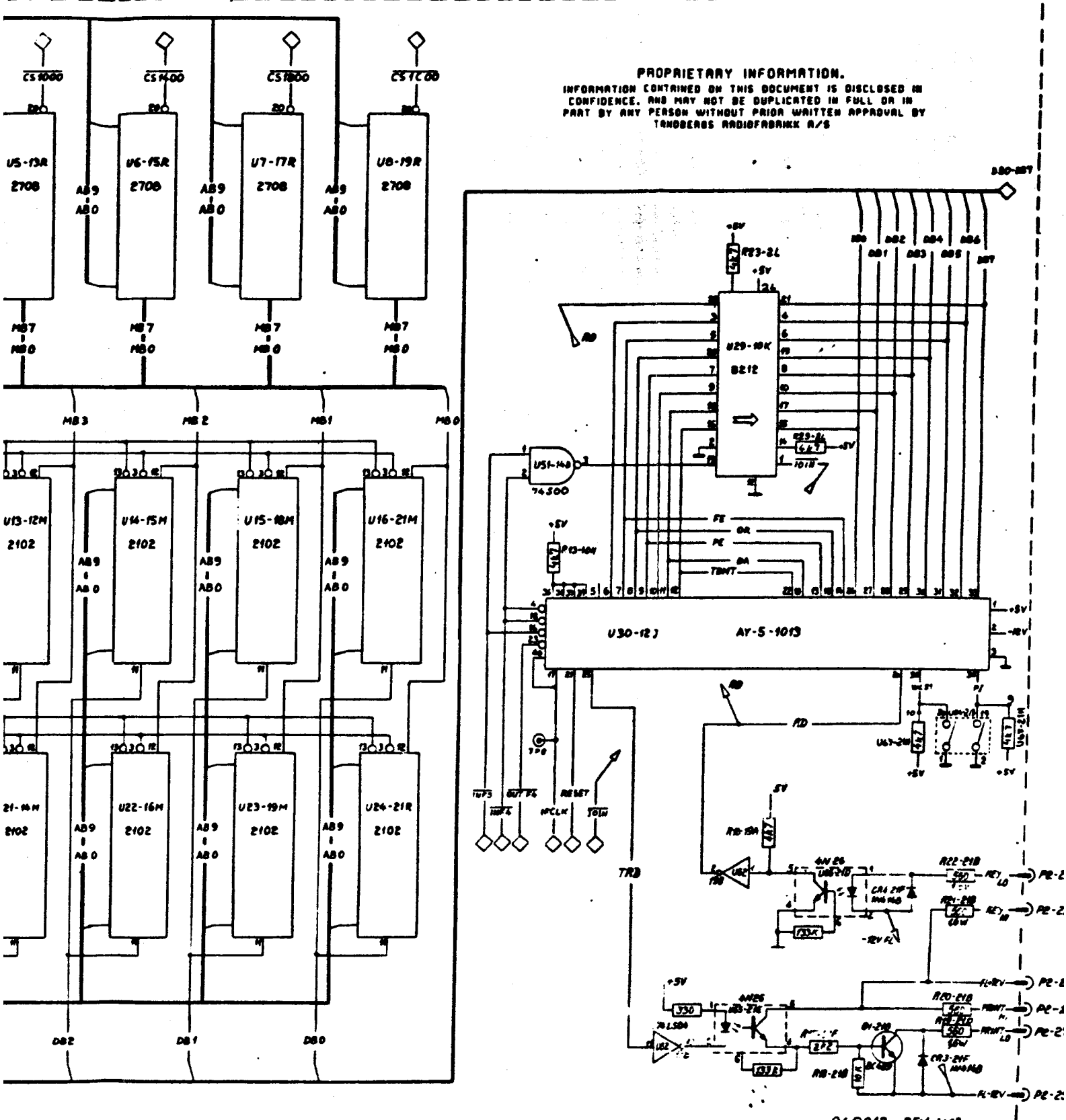

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6-12-76 BOB
20-6-78 Tech power