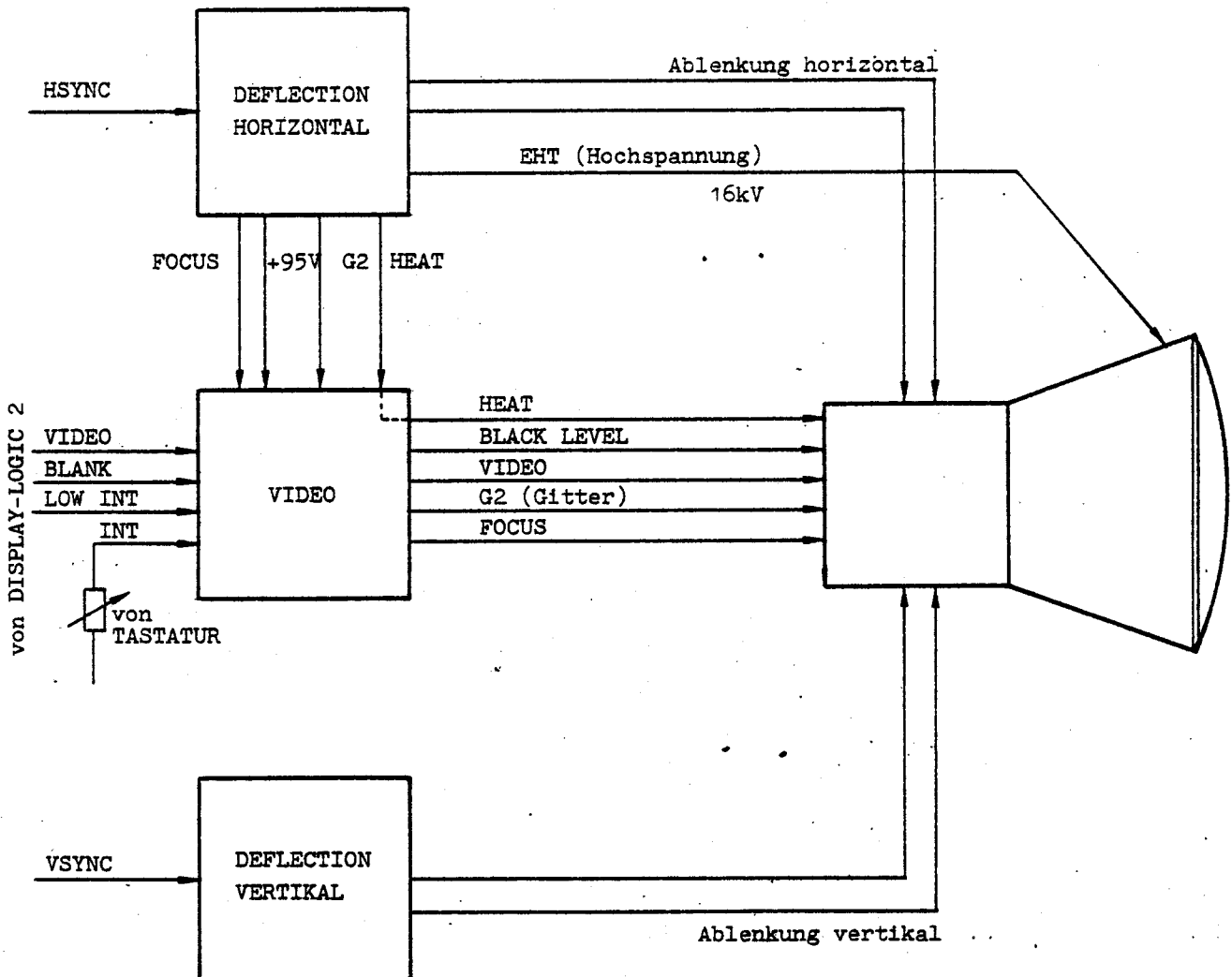


BLOCKSCHALTBILD



DEFLECTION HORIZONTAL

Das von der DISPLAY LOGIC 2 kommende Signal HSYNC synchronisiert einen Oszillator, der die Horizontalspannung erzeugt. Diese Spannung wird verstärkt und den Ablenkspulen zugeführt.

Außerdem werden hier die Hochspannung 16 kV und andere Hochspannungen für die Bildröhre erzeugt.

Es sind Einstellmöglichkeiten vorhanden für:

Horizontal Frequenz
Horizontal Liniarität
Fokusspannung

DEFLECTION VERTIKAL

Das von der DISPLAY LOGIC 2 kommende Signal VSYNC synchronisiert einen Oszillator, der die Vertikalsweep-Spannung erzeugt. Diese Spannung wird verstärkt und den Ablenkspulen zugeführt.

Es sind Einstellmöglichkeiten vorhanden für:

Vertikal Frequenz
Bildhöhe
Liniarität oben
" unten
Ruhestrom

VIDEO BOARD

Das VIDEO-Signal wird verstärkt und schaltet den Elektronenstrahl an und ab. Die Signale BLANK, INT und LOWINT steuern die Kathode und damit den Elektronenstrom.

Die Platine sitzt direkt am Röhrensockel. Über sie werden die Heizspannung und die Gitterspannung G2 dem Röhrenstecker zugeführt.

Es sind Einstellmöglichkeiten vorhanden für:

LOW INTENSITY
BLACK LEVEL

Signale zur Ablenk- und Videoelektronik

HSYNC: wird generiert nach jedem Horizontalzyklus um den Strahl Rücklauf einzuleiten (Horizontalrücklauf)

BLANK: Leucht-Unterdrückung während:
a) Strahl außerhalb des Bildbereiches
b) Strahl-Rücklauf

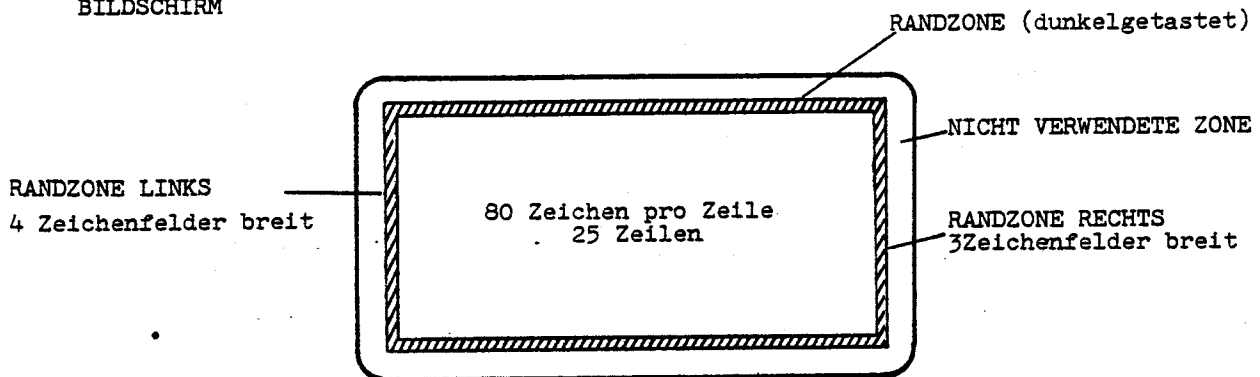
VSYNC: wird generiert, sobald der Strahl die rechte untere Bild-Ecke erreicht hat um den Rücklauf nach links oben einzuleiten (Vertikalrücklauf)

VIDEO: schaltet den Strahl aus/ein, um das Punkt-Muster zu erzeugen.

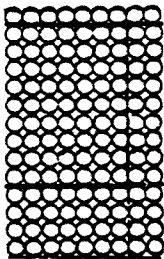
LOW INT.: wird erzeugt falls ein Attribut-Steuerzeichen "Halbhell" einem bestimmten Feld zugeordnet ist. Für diesen bestimmten Bildbereich werden die Zeichen mit niedriger Leuchtintensität abgebildet. (Niveau einstellbar)

INT.: Grundhelligkeit (von Tastatur (INTENSITY) aus regelbar)
(HELLIGKEIT)

BILDSCHIRM

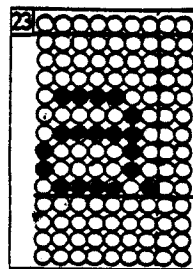
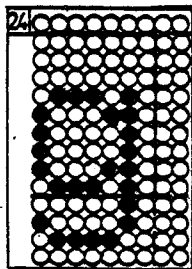
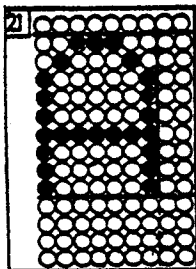


ZEICHENFELD



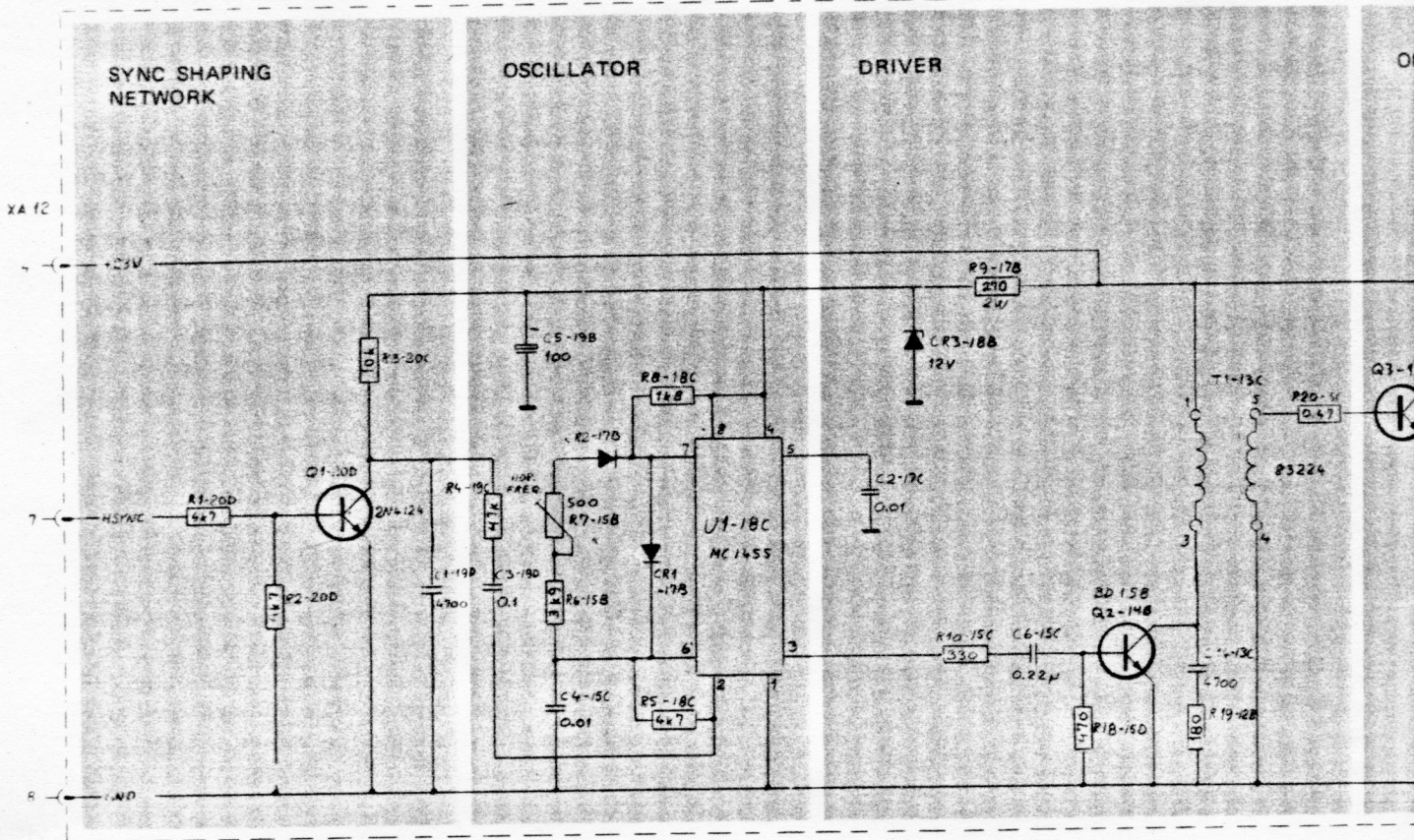
- Zeichenfeld 14 x 9 Bildpunkte
- Bildpunkt 9 wird ausgeblendet oder entspricht Bildpunkt 8 (Schalter auf Display Logik 2)

ZEICHENBEISPIELE

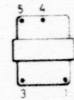


"STRICH-CURSOR"

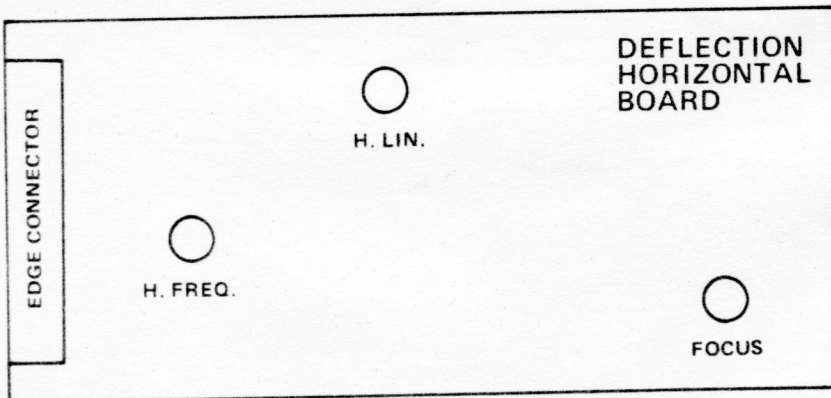
"UNTERSTREICHEN"



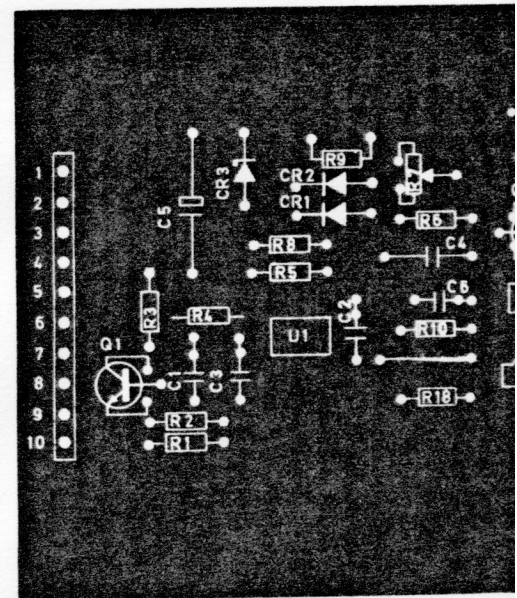
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BOTTOM VIEW OF
 TRANSFORMER T1

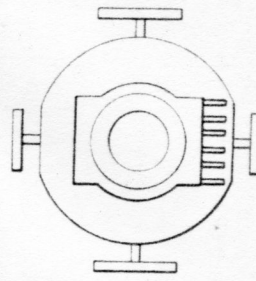
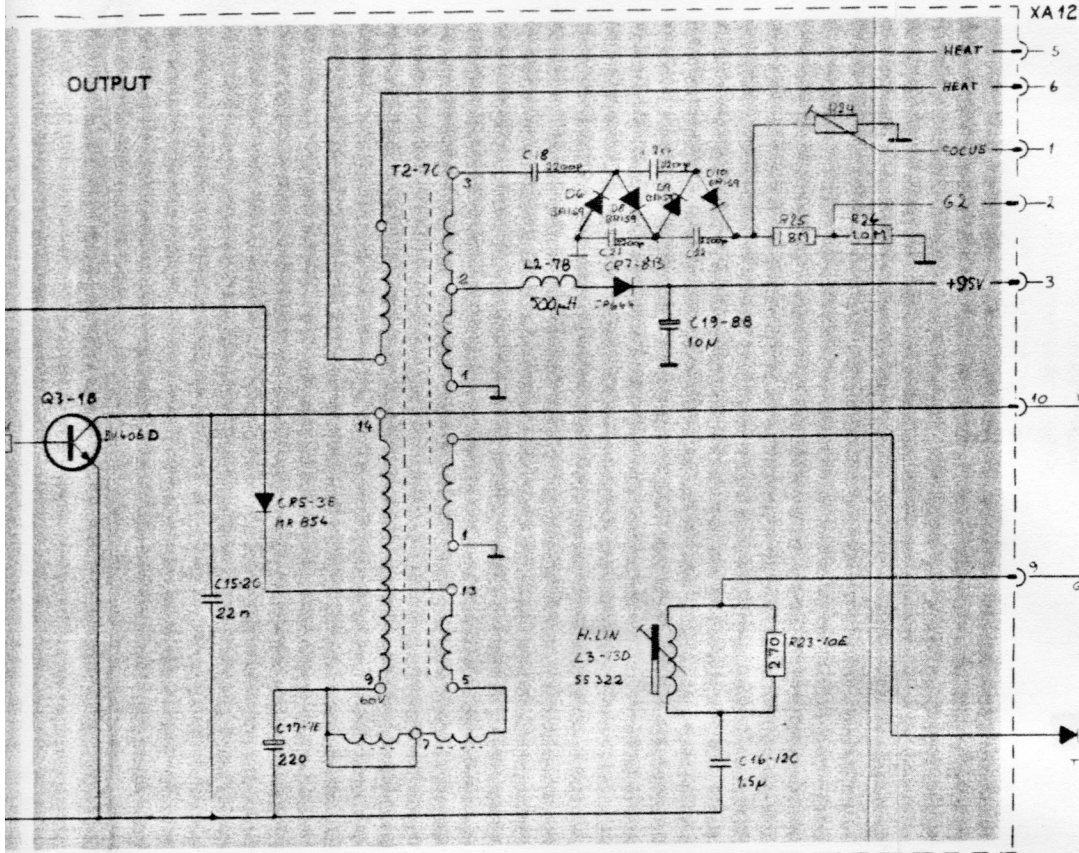


ADJUSTING POINTS ON THE HORIZONTAL DEFLECTION
 BOARD SEEN FROM THE SOLDERING SIDE



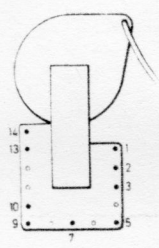
COMPONENT LO
 BOARD SEEN FR

*Auf Motherboard ist Angabe
 24V falsch \approx 23V*



DEFLECTION UNIT

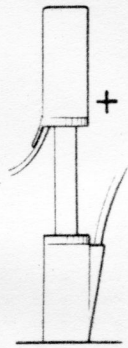
TV-18-2MT
ca. 16KV



BOTTOM VIEW OF TRANSFORMER T2

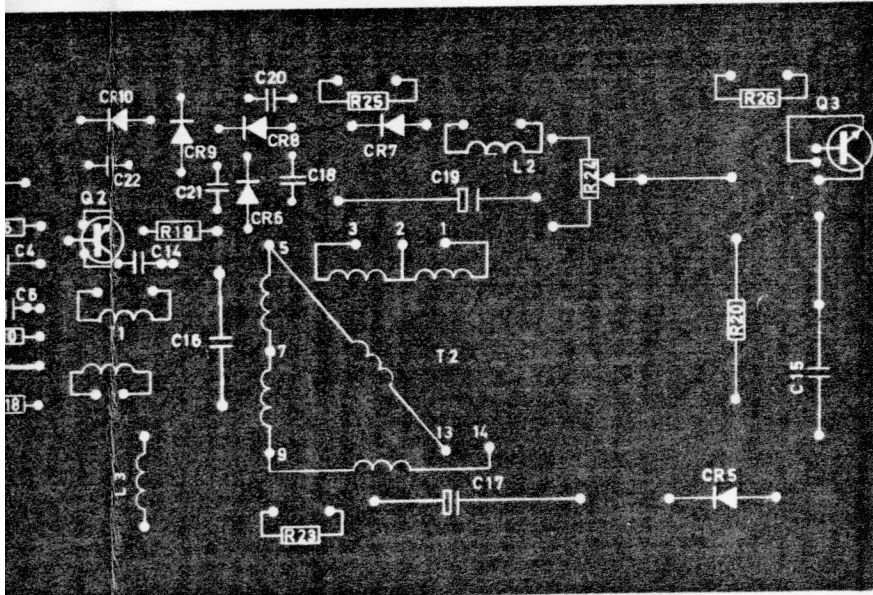
TO CAP ON RECTIFIER

FROM TRANSFORMER T2



RECTIFIER TV-18-2MT

TO PICTURE-TUBE (EHT)



COMPONENT LOCATION ON THE HORIZONTAL DEFLECTION SEEN FROM THE COMPONENT SIDE

Position	Name	Ordering No.	Rev. No.	Date
A12	Deflection Horizontal	960308	010	25.2.77

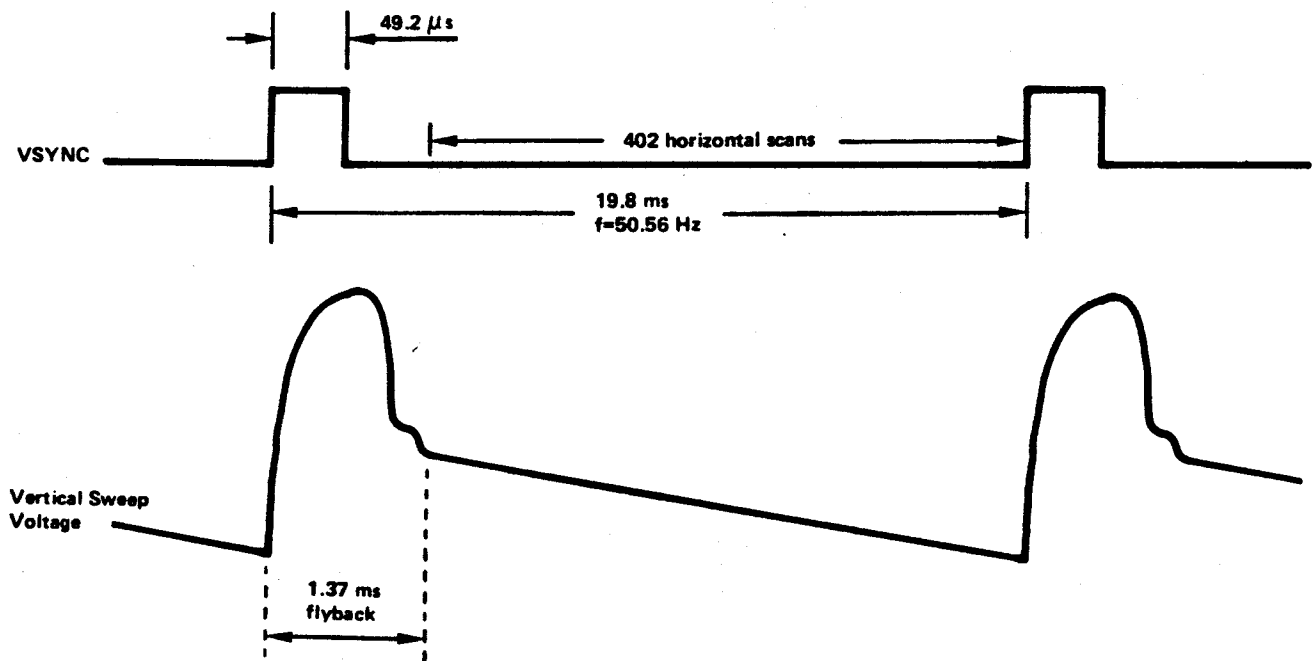
Deflection Vertical

The main function of the Deflection Vertical circuits is to generate an a.c. current in the vertical deflection coils mounted on the neck of the picture tube (CRT). The magnetic field resulting from this current moves the electron beam vertically on the screen. The current has sawtooth shape. When the sweep has reached the end of a scan it moves back to the starting position (fly-back) and starts a new scan.

An oscillator with approximately the correct vertical sweep frequency is triggered by the synchronization pulses (VSYNC) from the Display Logic 2 board. This means that even if the sync signal is missing the vertical sweep will continue, but it will not be synchronized.

The output voltage from the oscillator has sawtooth shape.

The figure below shows the relationship between the vertical synchronization pulses and the vertical sweep voltage.



DESCRIPTION OF THE SCHEMATIC

Sync Shaping Network

The vertical sync pulses (VSYNC) from the Display Logic 2 board are reshaped into sawtooth form by transistor Q1, resistor R2, and capacitor C2. C2 is charged through R2 and discharged through R3.

Oscillator

Thyristor Q2 works as a relaxation oscillator and is off during the time required to charge C5 through R8 and R9. When the voltage on the capacitor exceeds a certain level (i.e. the cathode of Q2 0.7 V lower than its gate) the thyristor turns on and discharges C5 rapidly. The thyristor turns off again when the discharge current fall below a critical value.

The freerunning frequency of the oscillator can be adjusted by potmeter R9.

Shaping Network

The amplitude of the deflection current and thereby the height of the picture may be adjusted with potmeter R10.

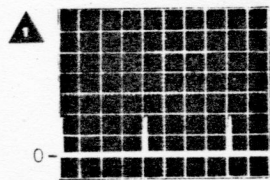
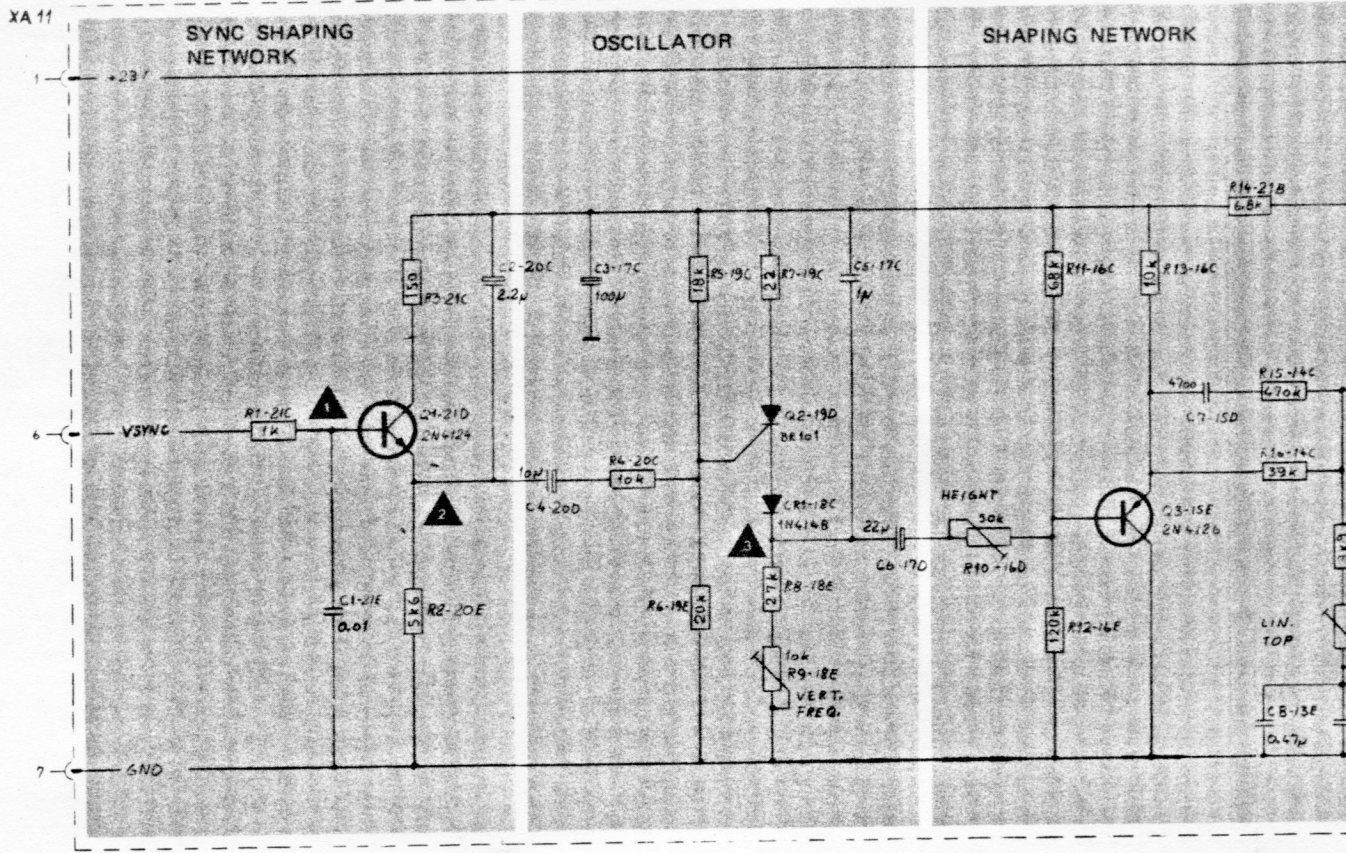
The components between the collector of Q3 and the base of Q4 determine the correct d.c. level at the base of Q4. The vertical linearity at the top of the picture may be adjusted with potmeter R18. These components influence the pulses at the beginning of the scan where the change in current is greatest.

Output Stage

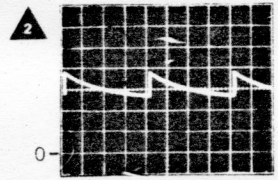
Transistor Q7 conducts the deflection current for one half of the vertical periode, Q8 for the other half. This results in an a.c. current in the vertical deflection coils. A quiescent current is needed to ensure a smooth overlap in switching points. This quiescent current may be adjusted with potmeter R25. Correct current is 10 to 20 mA in the transistors, if it gets higher the energy loss is too great, if it gets lower both transistors conduct simultaneously.

The vertical linearity at the bottom of the picture may be adjusted with potmeter R22 in the feedback circuit.

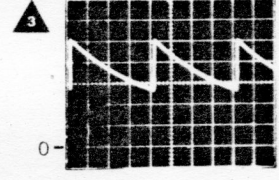
During flyback of the scan, when both transistors are in cut off, capacitors C10 and C11 together with the inductance in the vertical deflection coils form a tuned circuit. The flyback time may be changed by changing the values of C10 and C11.



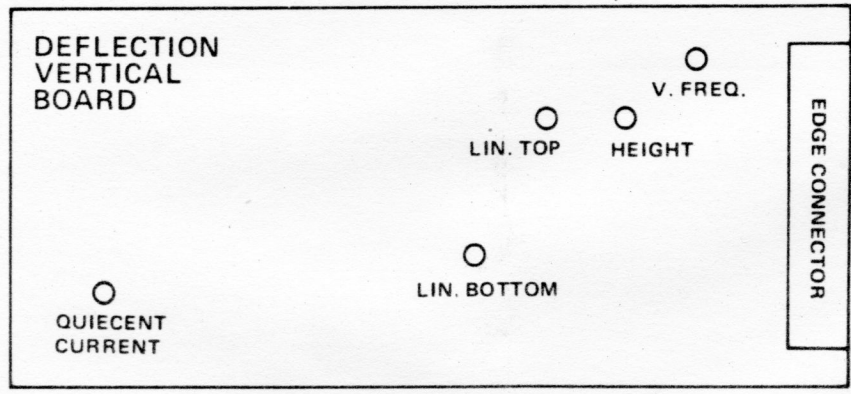
1 Y = 2 V/div
X = 5 ms/div



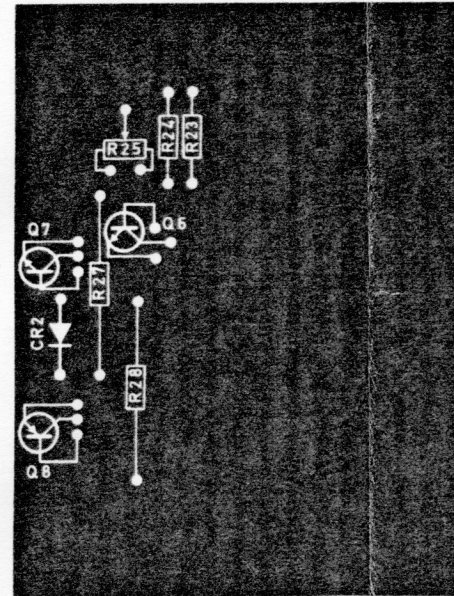
2 Y = 2 V/div
X = 5 ms/div



3 Y = 2 v/div
X = 5 ms/div

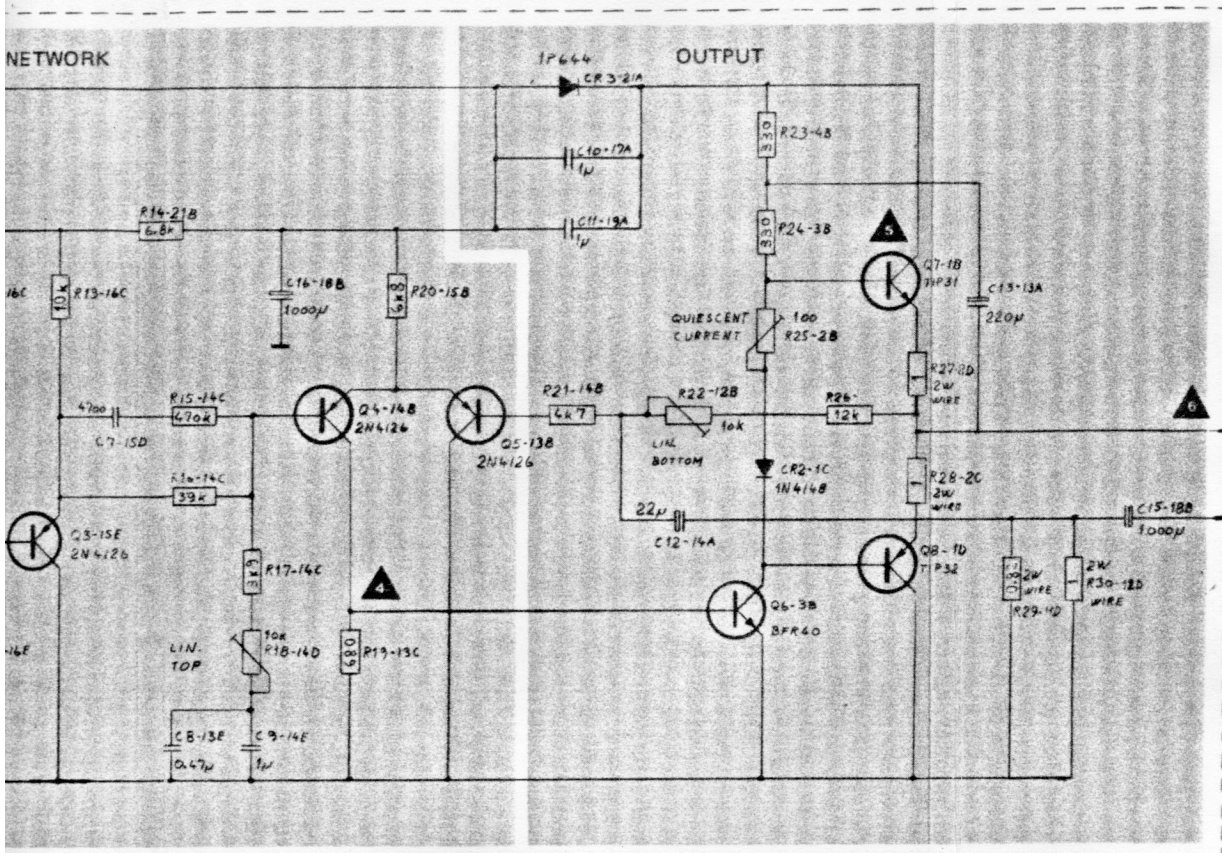


ADJUSTING POINTS ON THE VERTICAL DEFLECTION BOARD SEEN FROM THE SOLDERING SIDE

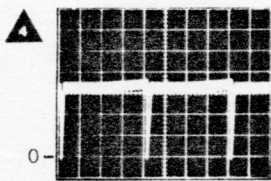


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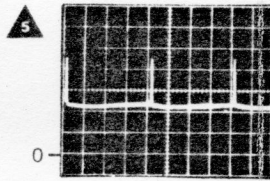
COMPONE
BOARD SI



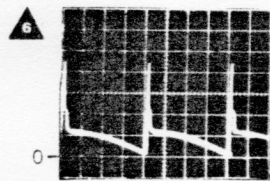
Y = 2 v/div
X = 5 ms/div



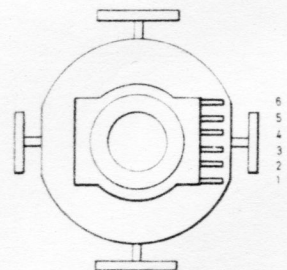
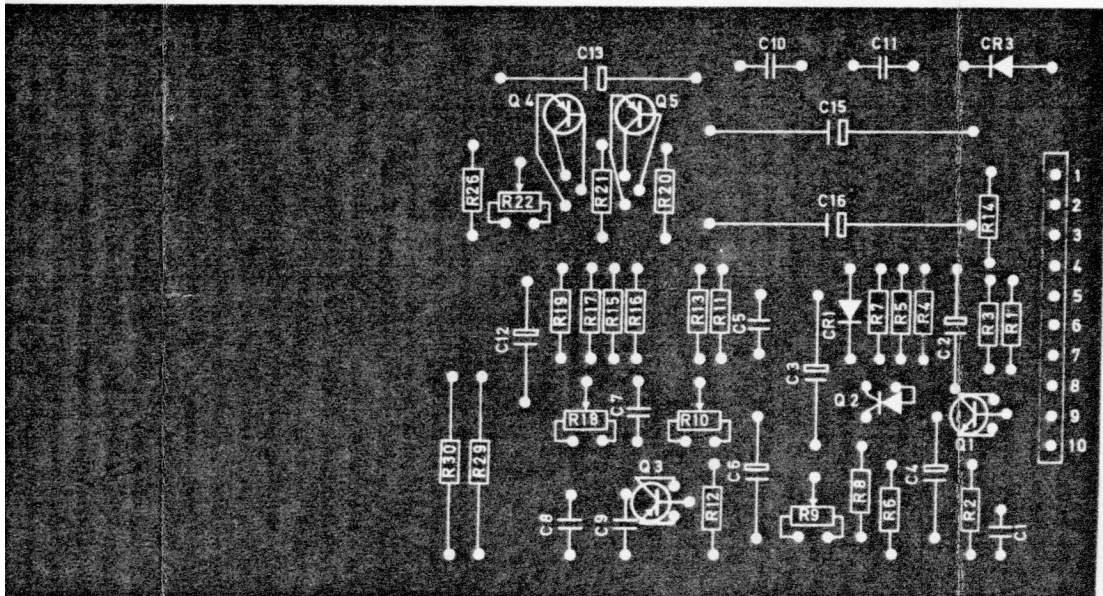
Y = 200 mV/div
X = 5 ms/div



Y = 10 V/div
X = 5 ms/div



Y = 10 V/div
X = 5 ms/div



DEFLECTION UNIT

COMPONENT LOCATION ON THE VERTICAL DEFLECTION BOARD SEEN FROM THE COMPONENT SIDE

Position	Name	Ordering No.	Rev. No.	Date
A11	Deflection Vertical	960307	010	7.3.77

DESCRIPTION OF THE VIDEO BOARD

Video Amplifier

The video signal from the Display Logic 2 board contains the information to be written on the screen of the CRT. This signal is fed from the driver Q1 to the emitter of the common base amplifier Q2 with about 40 times amplification. The output stage is made up of the complementary common emitter stage Q6 and Q7. The bootstrap circuit with Q8 increases the leading edge slope of the signal pulses.

Blanking Circuit

The electron beam in the CRT must be turned off, blanked, during flyback of the horizontal and vertical scans. The emitter of Q5 is high (TTL level) during blanking. Consequently R13 is no longer to ground and the CRT's cathode voltage increases to supply voltage (+95 V) high enough to turn the beam off. The desired black level of the CRT may be adjusted with potmeter R12.

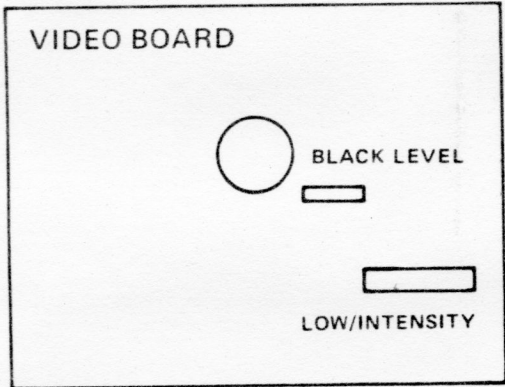
Intensity

The intensity of the picture may be adjusted by the 5k potmeter on the keyboard. This potmeter determines the voltage on the base of Q9 and in turn the voltage on the base of Q4. The resulting emitter voltage clamps the video signal to the level which corresponds with the desired intensity of the picture.

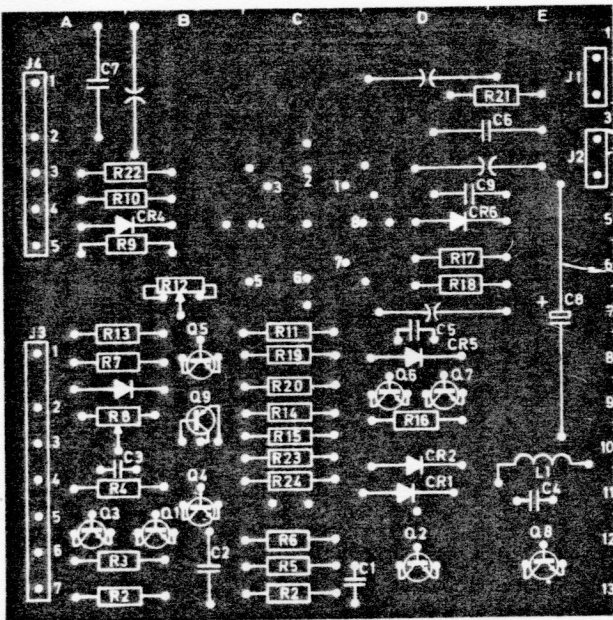
This level is further reduced when the attribute signal LOW/INT from the Display Logic goes true. This low level may be adjusted by potmeter R8.

CRT Circuits

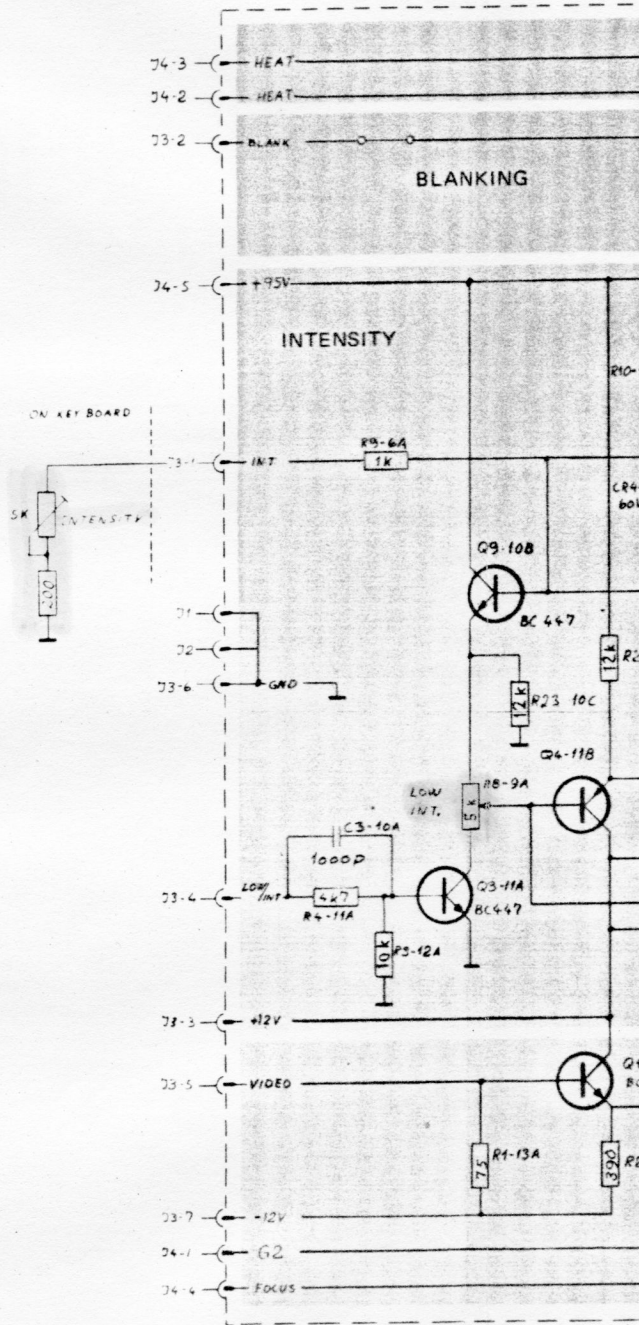
Resistors R19, R21 and R22 prevent high voltages caused by flash-over in the CRT from damaging other circuits. The spark gaps let high voltage transients to ground. Capacitors C6 and C7 are regular filter capacitors.

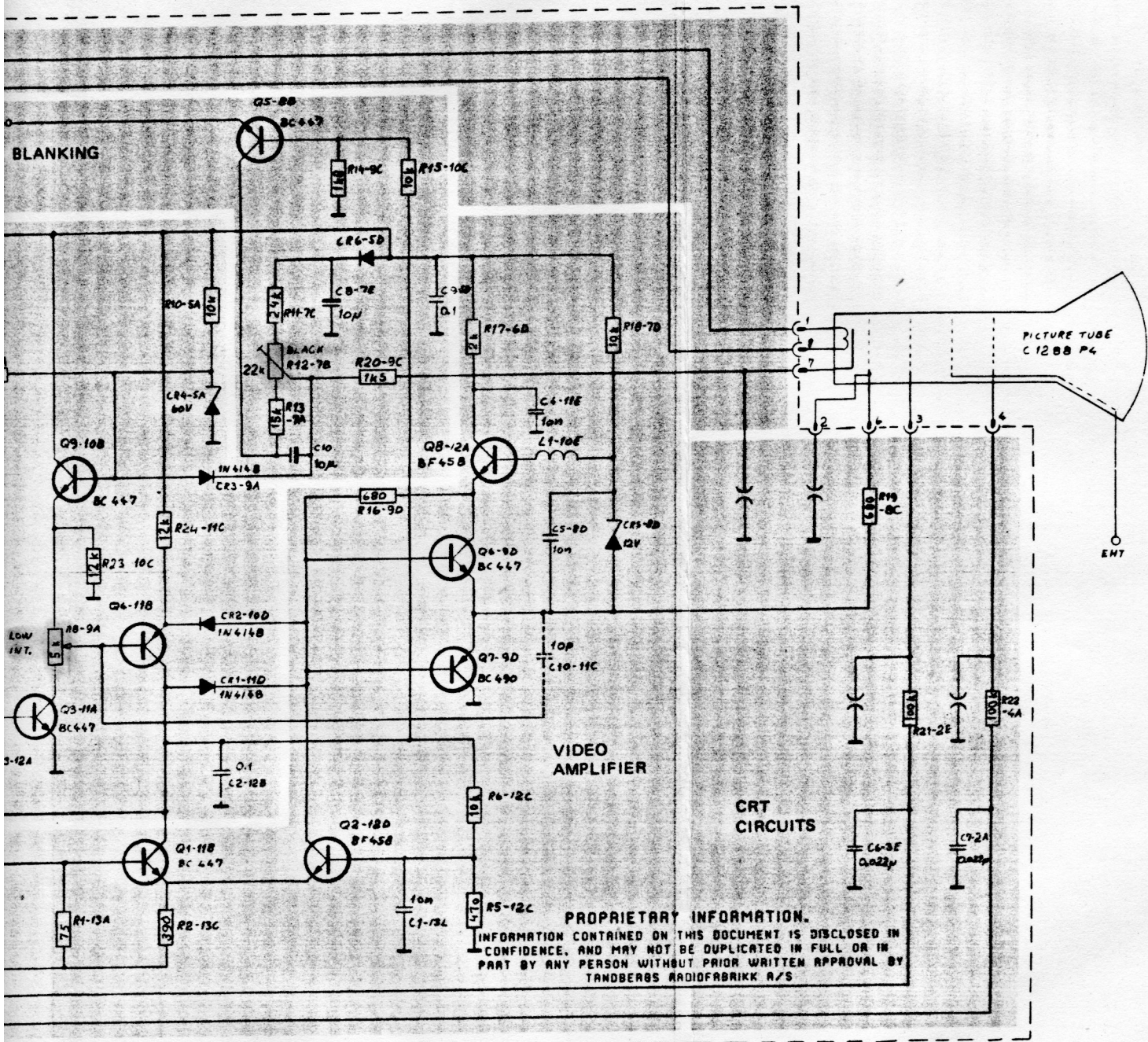


ADJUSTING POINTS ON THE VIDEO BOARD SEEN FROM THE SOLDERING SIDE



COMPONENT LOCATION ON THE VIDEO BOARD SEEN FROM THE COMPONENT SIDE

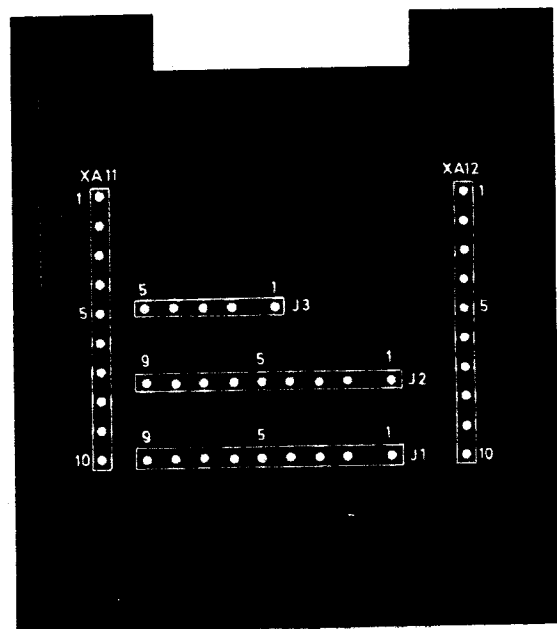
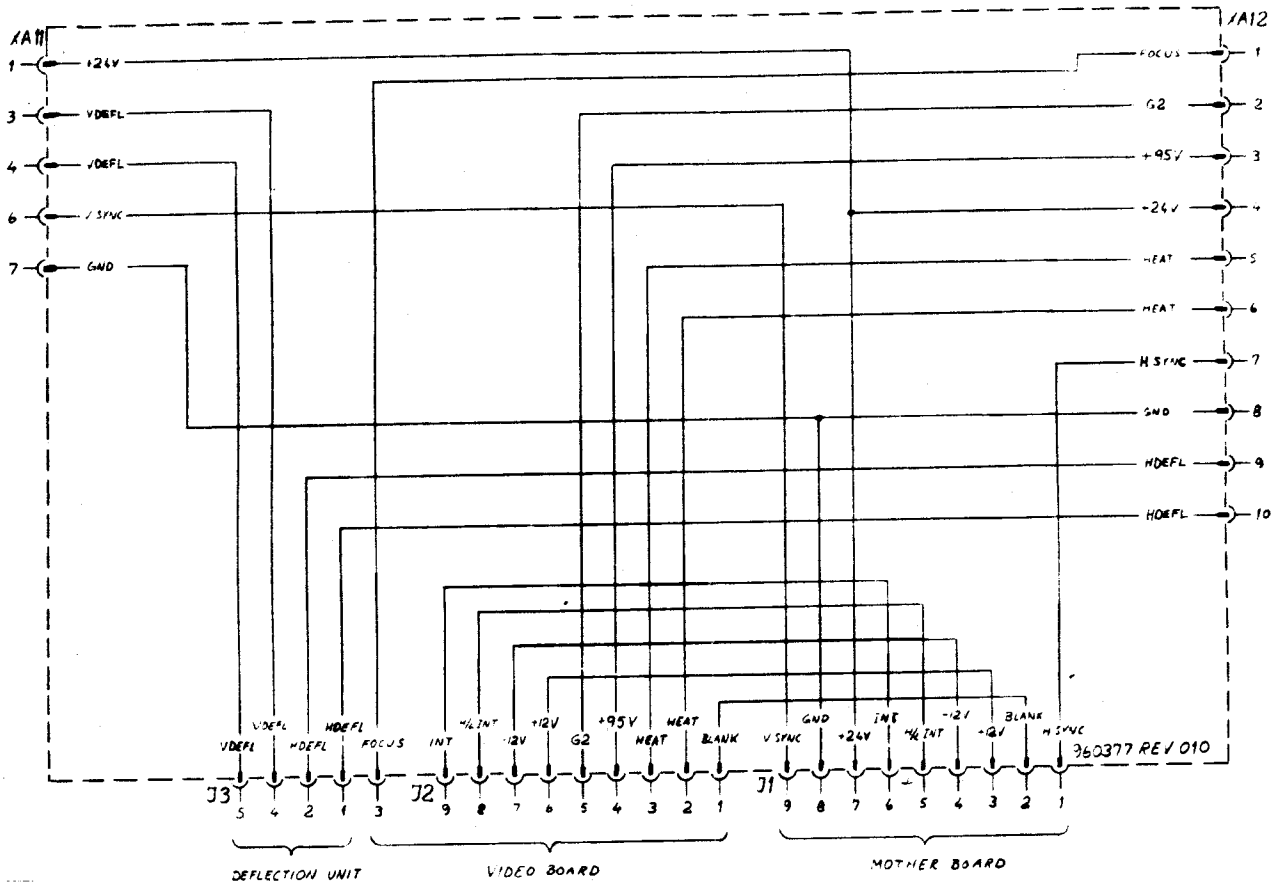




Position	Name	Ordering No.	Rev. No.	Date
A17	Video board	960306	011	16.4.77

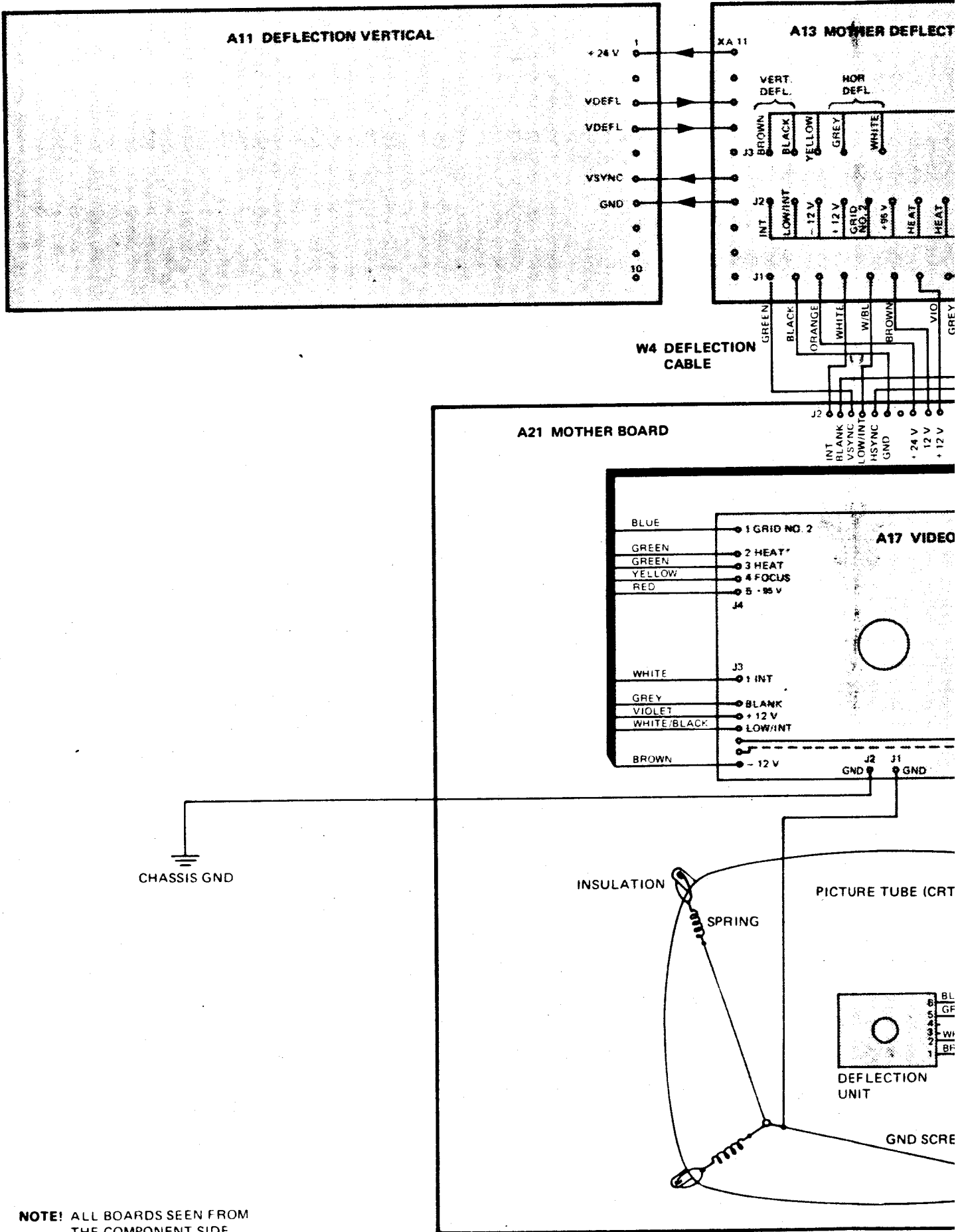
DEFLECTION
VERTICAL

DEFLECTION
HORIZONTAL

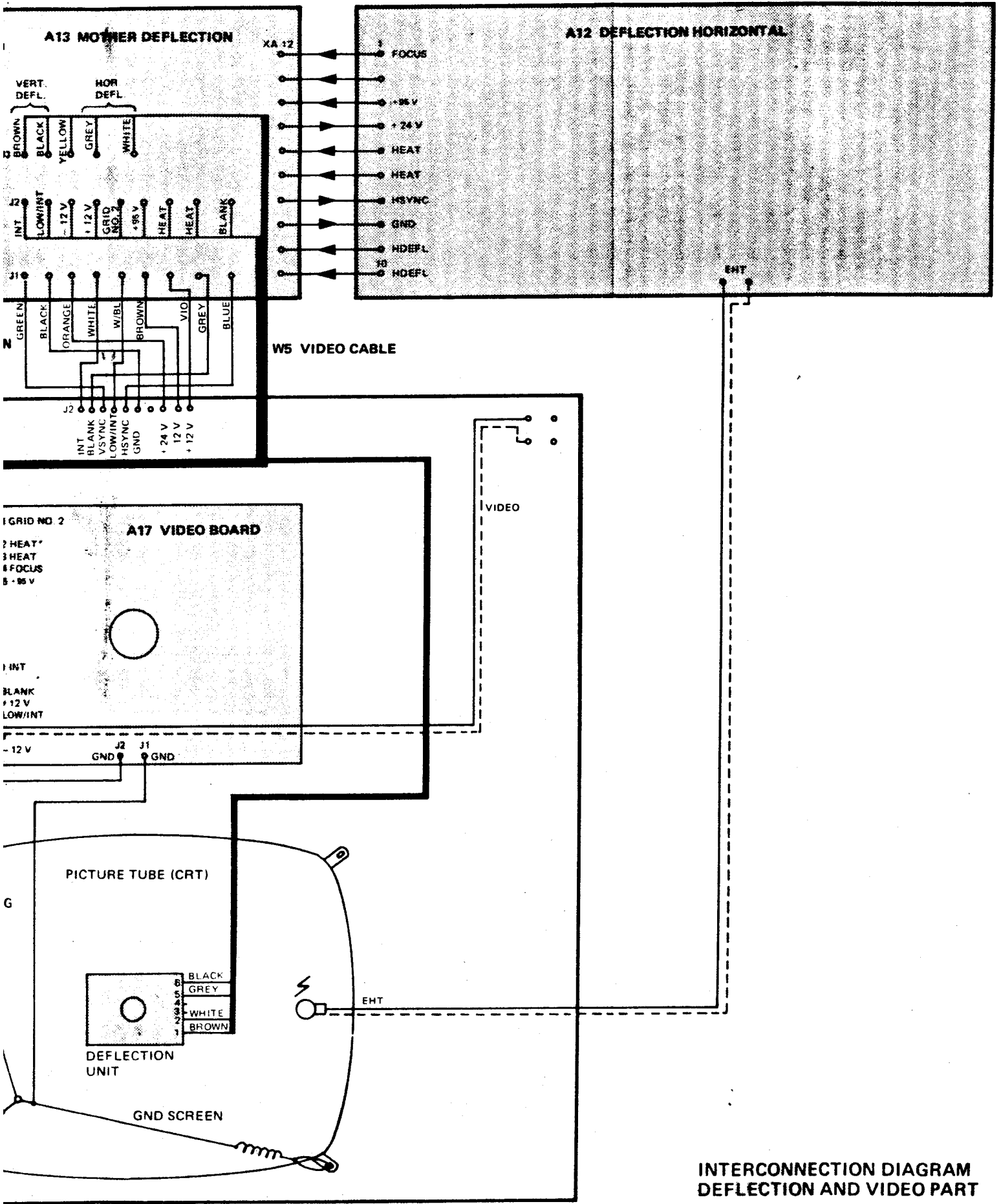


LOCATION OF THE CONNECTORS ON
THE DEFLECTION MOTHER BOARD
SEEN FROM THE COMPONENT SIDE

Position	Name	Ordering No.	Rev. No.	Date
A13	Deflection Mother	960377	010	26.2.77



NOTE! ALL BOARDS SEEN FROM THE COMPONENT SIDE.



INTERCONNECTION DIAGRAM DEFLECTION AND VIDEO PART