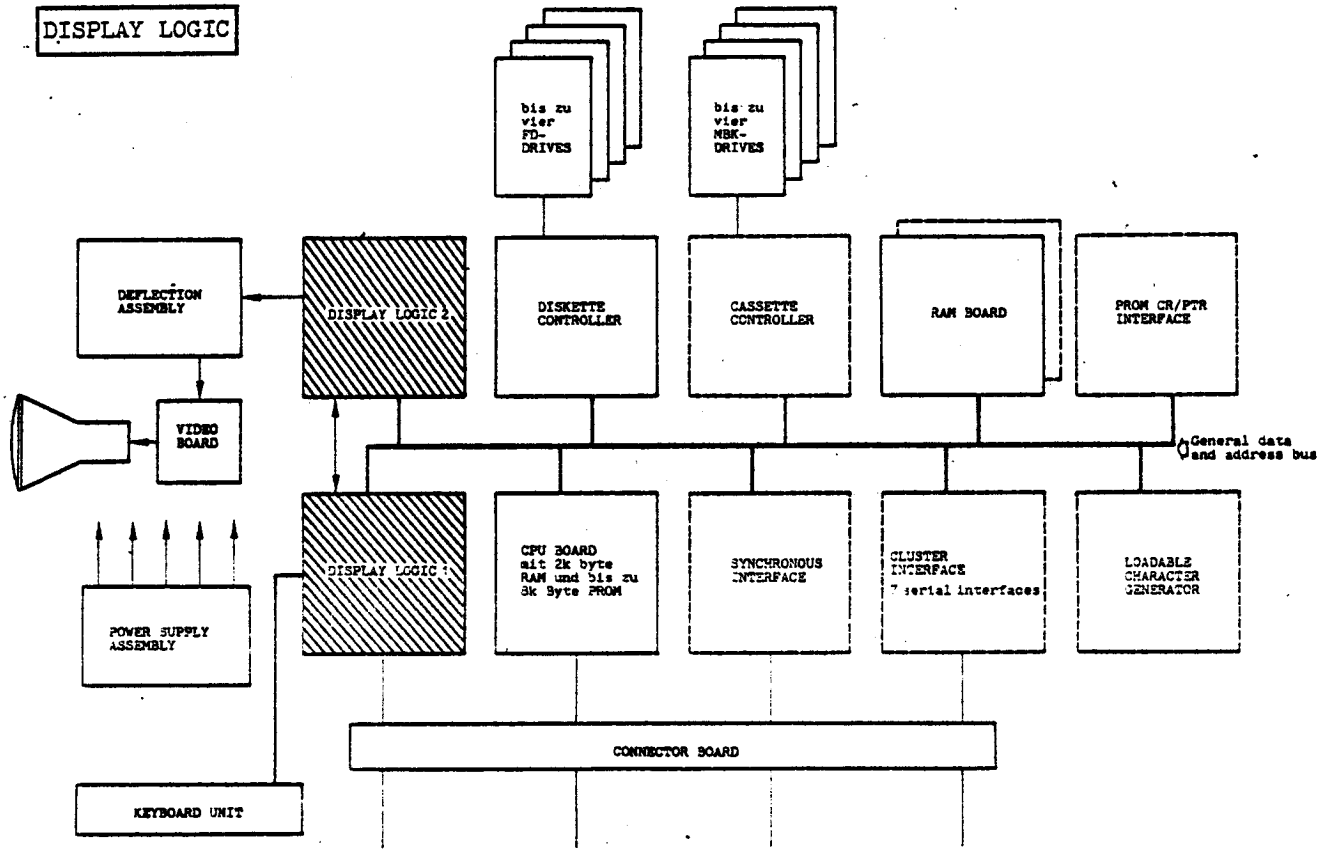
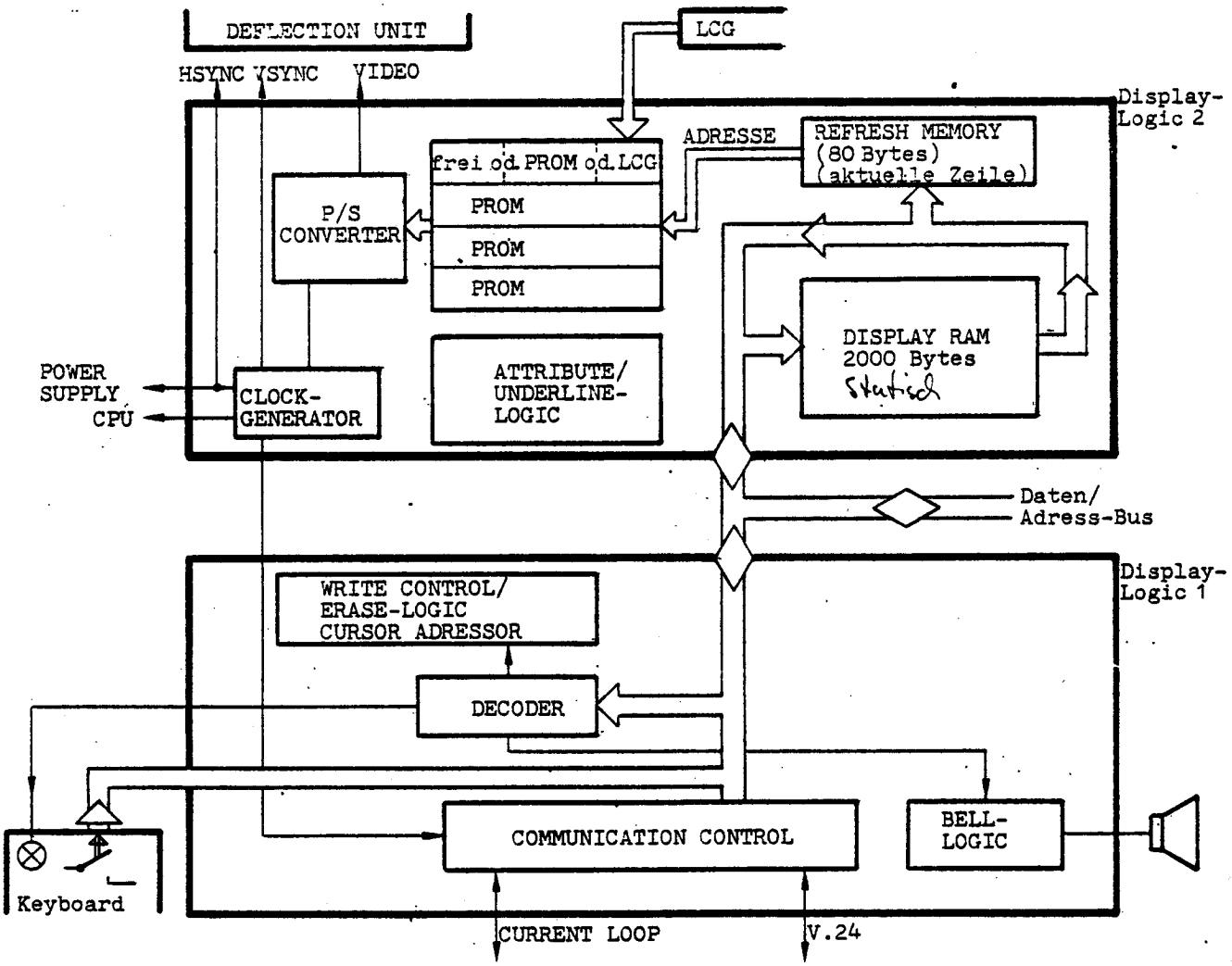
R E G I S T E R I

0	DISPLAY LOGIC I und II
1	Tastatur
2	Ablenkeinheit (Deflection Unit)
3	CPU (Central Processing Unit)
4	RAM (Arbeitsspeicher)
5	ROM (Festwertspeicher)
6	LCG (Loadable Character Generator)
7	Synchronous Interface
8	Cluster Interface
9	Stromversorgung

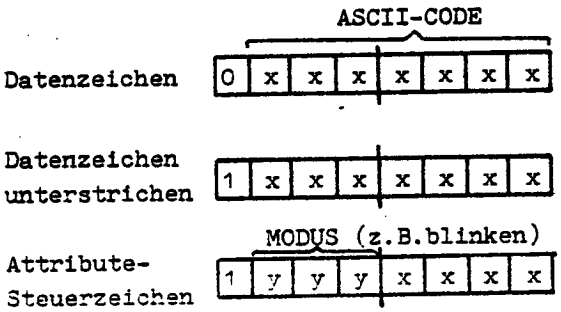


BLOCKSCHALTBILD



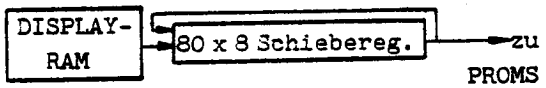
DISPLAY RAM

- 2 K x 8 Bit - Speicher
- 7 Bits für Daten
- 1 Bit zur Steuerung für Underline/ Attribute - Modus



REFRESH MEMORY

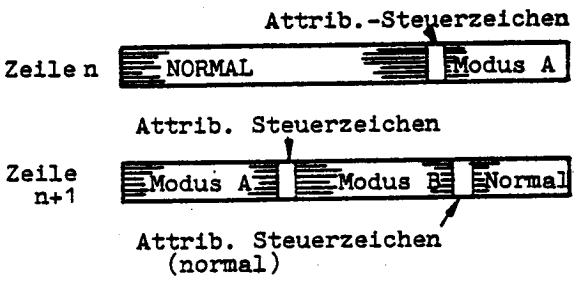
- Enthällt die ASCII-Zeichen der Zeile, die gerade auf der Bilröhre geschrieben wird. (aktuelle Zeile)



Die Daten kreisen 14 x (siehe Zeichfeld) Nach dem 14. "Shift" wird die nächste Bildschirmzeile vom Display-RAM nachgeladen.

ATTRIBUTE/UNDERLINE-LOGIK

1) Attribute Modus (Schalter S4 und S7 →ON)
Display logic 2



- Mit Attributsteuerzeichen kann die Darstellungsart von Feldern bestimmt werden.
- An der Stelle des Attrib. Stz. erscheint am Bildschirm ein "Blank" (Ausnahme s. Schalter 7 auf Display Logic 2)
- Der jeweilige Darstellungsmodus bleibt erhalten, bis ein neues Attrib.-Steuerzeichen folgt.
- Verfügbare Attribut-Modi

Modus	Steuerzeichen Kombin.	Abbildung wenn S7 OFF (nur bei Fehlerdiagnose)
INVERS VIDEO	1 1 0 0 0 0 0 1	A
BLINK	1 0 1 1 x x x x	Ziff 0-9
LOW INTENSITY	1 0 1 0 0 0 0 0	Space
UNDERLINE	1 1 0 1 0 0 0 1	Q
INVISIBLE	1 1 1 0 0 0 0 1	@
NORMAL	1 1 1 1 0 0 0 1	q

Für Kurzüberprüfung kann der Wartungstechniker og. Modi über Tastatur auswählen:

Modus	Tastenfolge	Hex-Code
Invers Video	Underline Shift A Normal	0E 41 0F
Blink	Underline bel. Ziff (z.B.0) Normal	0E 30 0F
LOW Intensity	Underline Space Normal	0E 20 0F
Underline	Underline Shift + Q Normal	0E 51 0F
Invisible	Underline a Normal	0E 61 0F
Normal	Underline q Normal	0E 71 0F

2) Underline Modus (Schalter S4 und S7 OFF)
Display Logic 2

Wird der Code "UNDERLINE ≙ 0E" zur Display-Logic gegeben, werden die Zeichen unterstrichen dargestellt. Mit dem Code "NORMAL ≙ 0F" wird Underline ausgeschaltet.

PROM

- Enthält das Bildpunkt-Muster
- max. 4 PROM-Bausteine à 32 Zchn steckbar.
- anstelle 4. PROM-Baustein ist ein ladbarer Zeichengenerator steckbar (seperate Baugruppe mit Zuleitung zum 4. Stecksockel auf Display Logic 2)

CLOCK GENERATOR

Grundfrequenz 20,2752 MHz
-Takt für Communication control (UART)
-Takte für Horizonal/Vertikal-Ablenkung
-Takt für CPU-Baugruppe

P/S-CONVERTER

-Konvertiert das paralell
angebotene Bildpunkt-Muster
vom PROM in Seriell-Information
(Video-Signal)

DECODER

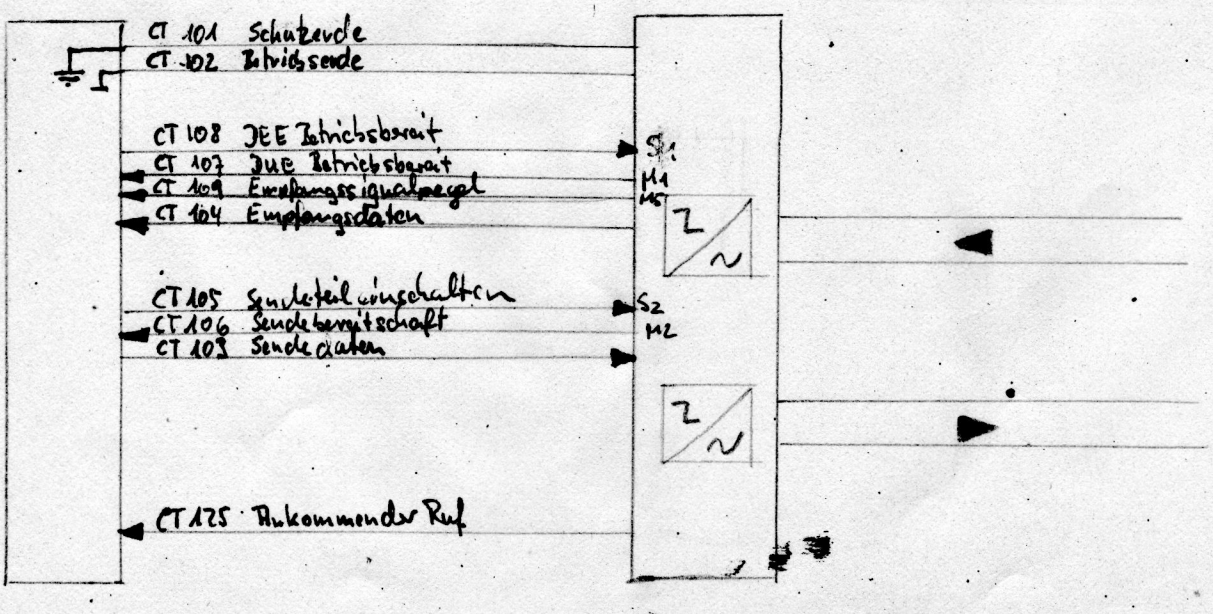
-Decodierung für Steuerzeichen
(siehe ASCII-Code-Tabelle)

WRITE CONTROL
ERASE LOGIC
CURSOR ADRESSOR

-Löschfunktionen
-Cursorpositionierung

COMMUNICATION CONTROL

-DFÜ-STEUERUNG ASYNCHRON
-Schnittstellenanpassung V.24
-Schnittstellenanpassung Current Loop
-Empfangs/Sendelogik
(UART-Baustein/
Universal asynchronuos receiver transmitter)



CIRCUIT DIAGRAMS

The circuit diagrams for Display 1 take up three sheets and the Display 2 diagrams take up four sheets.
To ease signal tracing, each diagram sheet carries a number framed with a diamond (e.g. ◇).
Signal lines entering or leaving a diagram sheet, but corresponding with another sheet of the same board are identified by the relevant "diamond reference".

CONNECT CONTROL

The main output signal of this block (CON) controls the data gates in the Data Flow Control and thus determines whether the unit will be connected to the remote computer or whether there shall be only a local data path. At the same time CON goes to the modem which responds by sending DSRD on circuit CT107 if the modem is ready for connection to the communication link. The WAIT light is on in the interval between CON and DSRD, and when CON goes true the ON-LINE light comes on. CON is switched between true and false by the LINE key or by the command CPLIN from the CPU which will both make the connect flip-flop toggle. If the switch U39 pin 6-15 is closed CON will go true when power is switched on. RCRDY enables the signal path for received data.

TRANSMIT CONTROL

The main output signals of this block are RQTS which is a request to the modem for permission to transmit, and TRRDY which when true enables the signal path for out-going data in the Data Flow Control. RQTS is switched on and off by TRANS key which makes the transmit flip-flop toggle. The command CPTRS from the CPU has the same effect. TRRDY however, can only be true when RQTS and RFS are true at the same time.

If switch U79, pin 2-19 is closed, the LINE key will have the same function as the TRANS key.

DATA FLOW CONTROL

Sets up the signal paths for serial data from the SO output of the UART and back to its SI input. In local mode (CON false) or with internal echo (EXTE false) the data path goes via U64-9. The path for incomming data is inhibited by the false RCRDY at U65-5 and the out-going path is inhibited by the false TRRDY at U65-12.

The local path will be broken in On-Line mode by CON which is then true and inhibits U51-13 unless the echo switch on the switch panel is set for internal echo (EXTE false).

The opto-couplers U77 for the receiving current loop and U78 for the transmitting current loop provide galvanic isolation between the current loop and the rest of the terminal. The signals are carried through the coupler by the light emitted from the light diode and picked up by the photo-transistor.

WRITE CONTROL

The main purpose of the \
enables the Display RAM

When it has been decided
written into the Display R
from the CPU) RAMWRP

If the character is a DLE c
RAMWRP.

DLE also tells that the tw
Cursor Counters as addres
Control generates a SETC
by making DISCTR true a
CURAD is generated both
when the CPU wants to re
ments the Horizontal Curs
reading and writing is that
these operations. In other
flip-flop U58-2 is set and
MBSYIR from the flip-flo

CPU COMM

Command
from the C
Bus are dist
these gates
is true.

INTERFACE STATUS

Status signals from the
CPU are transmitted on
from this Port when IO
are true.

display-

WRITE CONTROL

The main purpose of the Write Control is to generate the RAMWRP which enables the Display RAM (Display 2) for writing-in.

When it has been decided that the code on the data bus is a character to be written into the Display RAM (TURDEC true or write command CRAW from the CPU) RAMWRP goes true.

If the character is a DLE code the NONWR signal will inhibit generation of RAMWRP.

DLE also tells that the two following characters are to be loaded into the Cursor Counters as address for the Display RAM. In that case the Write Control generates a SETCC signal for the Cursor Addressor which responds by making DISCTR true and thus disabling the decoder (CTRLEN false). CURAD is generated both during a write operation (RAMWRP true) and when the CPU wants to read from the RAM (RINPEN true) and it increments the Horizontal Cursor Counters. An absolute requirement for both reading and writing is that the RAM is not already carrying out one of these operations. In other words MBSY must be false. If MBSY is true, the flip-flop U58-2 is set and if then a write or read command arrives, the MBSYIR from the flip-flop will activate the Interrupt Generator.

CPU COMMAND GATES

Command signals received from the CPU via the Data Bus are distributed from these gates when IFCOM is true.

CURSOR ADDRESSOR

When a DLE character is decoded it means that the two characters to follow are to be loaded into the cursor counters as an address for the RAM. The preset input of flip-flop U44-4 goes low for a moment at the trailing edge os SETCC, switching the flip-flop to its set state so that DISCTR goes true and prevents decoding of the next characters. When SETCC goes true the next time, LVC will enable the load inputs of the Vertical Cursor Counter because U44-8 now is high. U44-11 is clocked by the trailing edge of LVC when SETCC is over, and hence U44-8 goes low. During the next character SETCC will make LHC go true and cause loading of the Horizontal Cursor Counter.

The trailing edge of LHC clocks U44-3 which returns to its reset state and makes DISCTR false so that the next character is dealt with in the normal way.

INTERFACE STATUS PORT

Status signals from the Interface to the CPU are transmitted on the Data Bus from this Port when IOIN and IFST are true.

INTERRUPT CONTROL

Generates an interrupt request IREQ3 to the CPU when one of the following signals go

UART DA:	Data is ready at the UART output buffer.	
KBDA:	Data is ready at the keyboard port.	Only one of these signals will be allowed to interrupt at a time.
MBSYIR:	The CPU has tried to write into or read out of the RAM.	
CI:	Calling signal via modem from remote computer.	
TBMTIR:	The CPU wants to send data by an output instruction.	

When the CPU has acknowledged the interrupt request, it applies IOIN and ISTWD to t Status port U6 which will let the interrupt status word through to the data bus.

IACK3 is the response from the CPU telling that it is carrying out the requested interru interrupt requests on this level can be generated as long as IACK is true.

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2) for writing-in.

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RDEC true or write command CRAW

IONWR signal will inhibit generation of

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ATES
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Bus
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CURSOR ADDRESSOR

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The trailing edge of LHC clocks U44-3 which returns to its reset state and makes DISCTR false so that the next character is dealt with in the normal way.

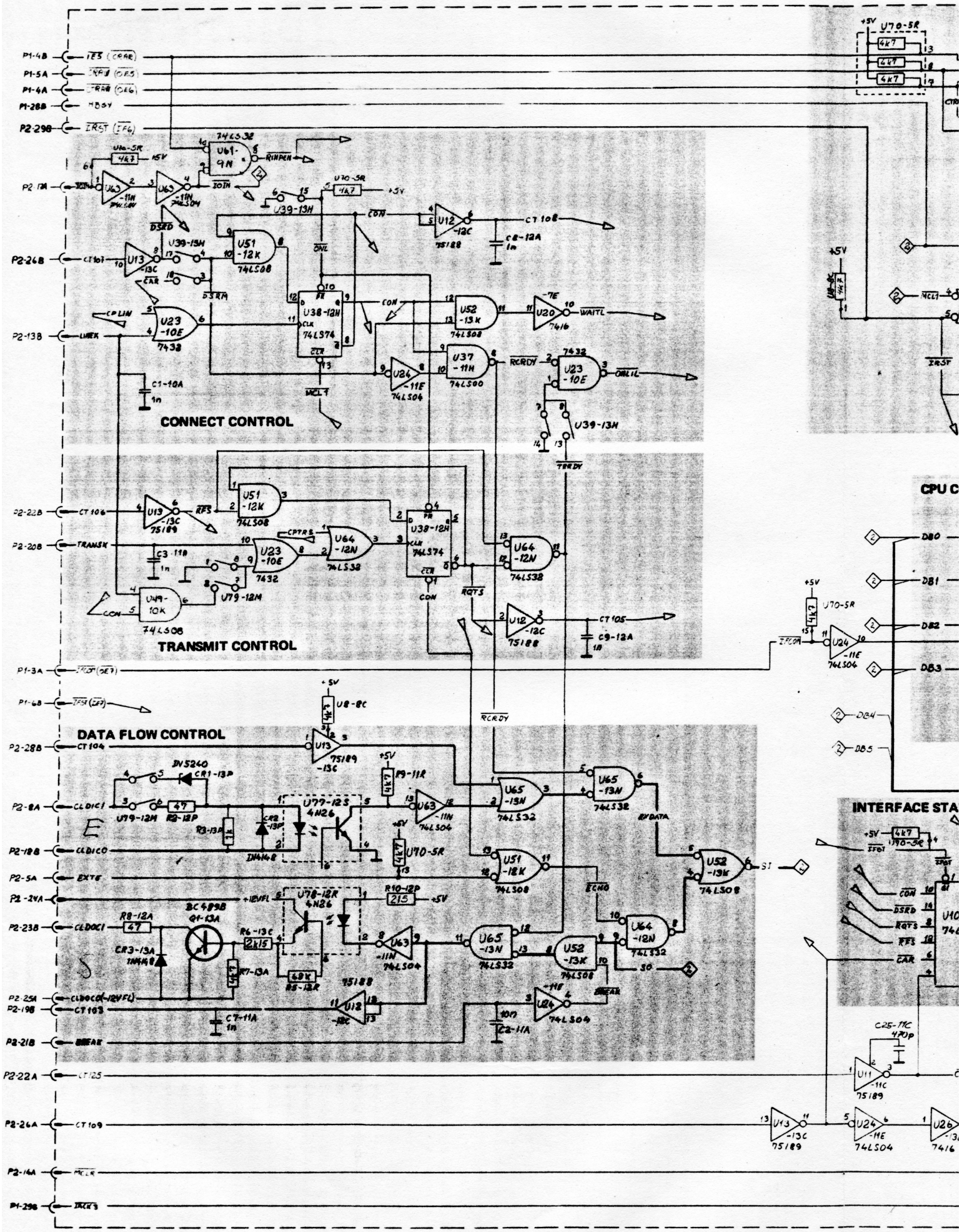
INTERRUPT CONTROL

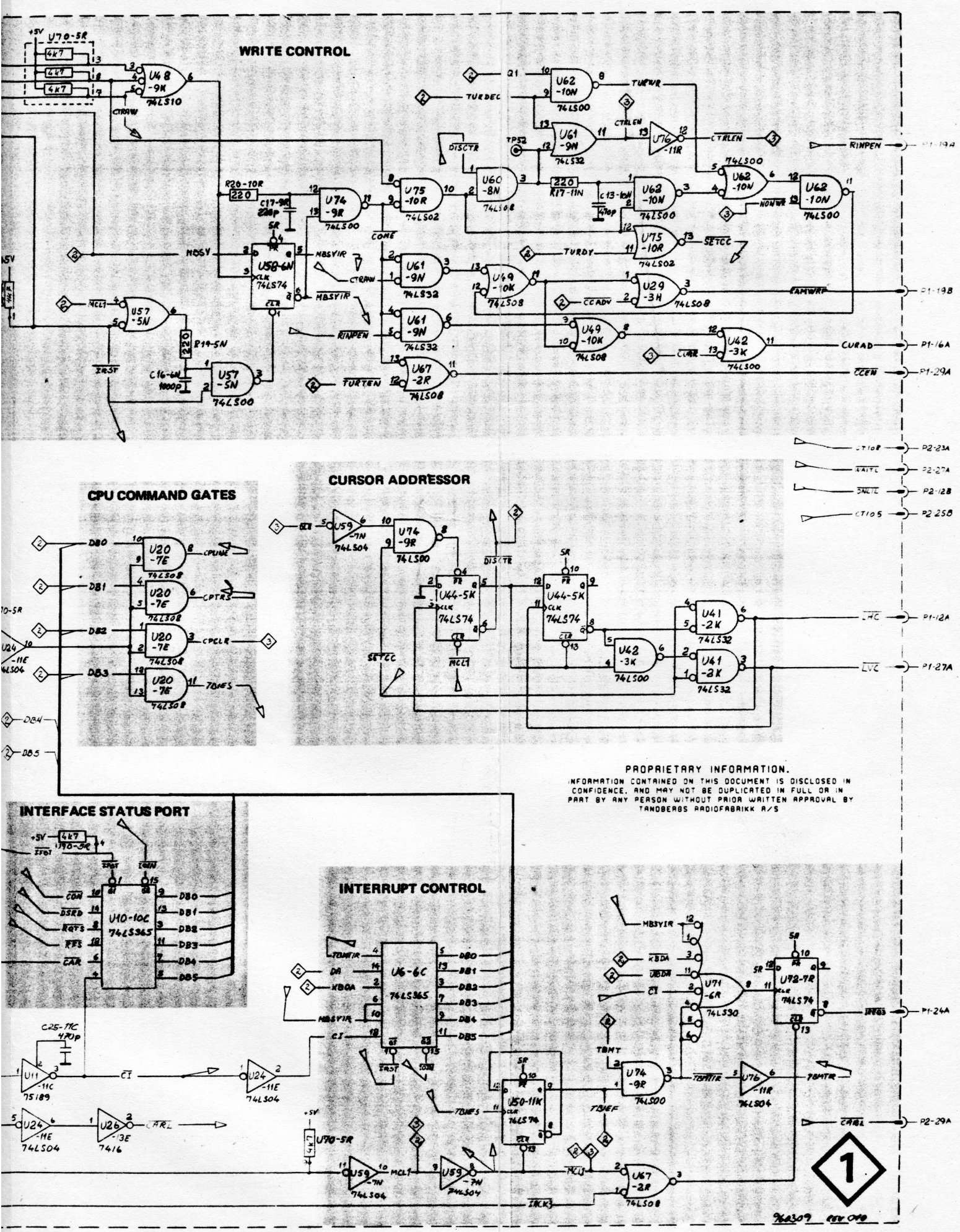
Generates an interrupt request IREQ3 to the CPU when one of the following signals goes true:

UART DA:	Data is ready at the UART output buffer.	
KBDA:	Data is ready at the keyboard port.	Only one of these signals will be allowed to interrupt at a time.
MBSYIR:	The CPU has tried to write into or read out of the RAM.	
CI:	Calling signal via modem from remote computer.	
TBMTIR:	The CPU wants to send data by an output instruction.	

When the CPU has acknowledged the interrupt request, it applies IOIN and ISTWD to the Interrupt Status port U6 which will let the interrupt status word through to the data bus.

IACK3 is the response from the CPU telling that it is carrying out the requested interrupt. No further interrupt requests on this level can be generated as long as IACK is true.


CONNECT CONTROL
TRANSMIT CONTROL
DATA FLOW CONTROL
INTERFACE STA
CPU C
See TIMING DIAGRAM 1 page 41.


WRITE CONTROL
CURSOR ADDRESSOR
CPU COMMAND GATES
INTERFACE STATUS PORT
INTERRUPT CONTROL
PROPRIETARY INFORMATION.
INFORMATION CONTAINED ON THIS DOCUMENT IS DISCLOSED IN CONFIDENCE, AND MAY NOT BE DUPLICATED IN FULL OR IN PART BY ANY PERSON WITHOUT PRIOR WRITTEN APPROVAL BY TANDBERGS RADIOFABRIKK A/S
DISPLAY 1
display–27

UART CLOCK GENERATOR

The counter U46 has two different division rates depending on the setting of the Band Rate Switch. When the switch is in one of the positions 1 to 7, the counter is loaded by 5 giving a division by 11. When the switch is in position 0, the counter is loaded by 1 giving a division by 15. The resulting signal is taken through the divider chain U22 which feeds into the line selector U21. The binary value of the signals OCT A, B, and C from the Band Rate Switch determines which one of the counter outputs that is selected to be the URCLK signal appearing at TP53.

Division rates and URCLK frequencies for the various settings of the Band Rate Switch will appear from the table:

Switch	Division in: U46	U22	ERCLK frequency
0	15	256	110 Hz
1	11	128	300 Hz
2	11	64	600 Hz
3	11	32	1.200 Hz
4	11	16	2.400 Hz
5	11	8	4.800 Hz
6	11	4	9.600 Hz
7	11	2	19.200 Hz

The DOTCLK signal is also divided by 11 in U9 and then by 2 in U50 to give the Q1 signal at U50-5 (307200 Hz). This signal is used in the Bus Control and the Write Control. It is also fed via the CPU bus to the CPU board and to some interface boards.

CPU ENABLE GATES

Applies control signals to the Bus Control when IOIN is true.

BUS CONTROL

Assuming that the terminal is operating in the TTY mode (without CPU) a character code on the data bus from the keyboard is always accompanied by KSTR at U68-3 which will set U68-5 making KBDA true. If the transmitter buffer in the UART is empty (TBMT), U68-12 is set on the first positive edge of Q1 provided that flip-flop U66-5 or U66-9 is not already set by data from the UART and consequently TTKSTB goes true. This will in turn generate KBEN which enables the Keyboard Port and applies the character to the Data Bus. As KBEN goes true it resets KBDA which no longer has any function. KBEN also makes URLD true and thus loads the character on the Data Bus into the UART buffer. In the UART the data is transferred from the transmitter buffer register to the transmitter register when this is empty, and appears in series form at the SO output from where it goes to the Data Flow Control.

Received or echoed serial data appears at the S1 input of the UART and when a full character has been received URDA goes true.

If now another keyboard strobe has not arrived, KBDA is false and URDA will be let through from U57-9 and be clocked into U66-5 by the clock Q1. This will in turn cause URDEN to go true and enable the UART Data Buffer to let the character on to the bus.

Should data from UART and keyboard arrive at the same time, the keyboard data will have priority because U57-8 will let URDA through only when KBDA has not been allowed to give a logic 0 at U57-10. Even if KSTR arrives after URDA, but before flip-flop U66-5 is set, the keyboard will have priority. However, when U66-5 or 9 is set, TURTEN will inhibit TTKSTB. When URDEN goes true it also resets URDA to avoid an OE (overrun error) from the UART at the next character.

When the local CPU is incorporated the signals CPENKB, CPURLD, and CPUREN control the data bus and TTKSTB, TURDY, and TURDBC are then false.

ERASE LOGIC

Erase page is started by ERPAG, and erase line by ERLIN. They will both make the ERASE signal true and thus clamp the inputs of the RAM at binary 0. ERASE will also set U27-9 at the first CHCLK1 pulse to make ERDEL true and prepare U27-5 to be set at the trailing edge of HSYNC. Provided TREN is false (not scan 13) EREN goes true and lets CHCLK1 generate the CCADV signal which serves as write pulses and steps the horizontal cursor counter through the scan. EREN is also used by U30 and causes U31-4 to be reset at the next leading edge of HSYNC if it is an erase line operation or U31-9 to be reset at the trailing edge of DEC25 if it is an erase page operation. In scan 13, however, EREN is inhibited by TREN being true. Hence, CCADV is not generated during this scan and flip-flops U31 remain in their set state.

EL will immediately make RESCC true and reset the Horizontal Cursor Counter. EOP (erase page) will make HOME true and reset the Horizontal as well as the Vertical Cursor Counter.

KEYBOARD PORT

Enabled by KBEN to let a character from keyboard through to the data bus.

WRITE GATES

The ERASE signal is normally false and enables the gates so that data from the data bus is let through to the RAM. During an erase operation ERASE is true clamping all bits on the data bus at 0.

UART

Data from the data bus applied to the parallel inputs of the UART is converted to series form and appears at the S0 output as serial data to be fed to the remote computer via the Data Flow Control. Data received from the remote computer in series form is applied to the S1 input of the UART and appears at the parallel outputs. URDA tells when data is available from the UART and remains true until reset by URDEN. The status signal TBMT tells when the UART is ready to receive another character at the parallel inputs.

UART DATA BUFFER

Enabled by URDEN to let data from the UART in to the data bus.

UART STATUS BUFFER

Used by the CPU to supervise the status of the UART in order to control the data flow to and from it. The CPU requests status word by applying URSTIN and IOIN.

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ı Bus into the UART
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UART Data Buffer to let

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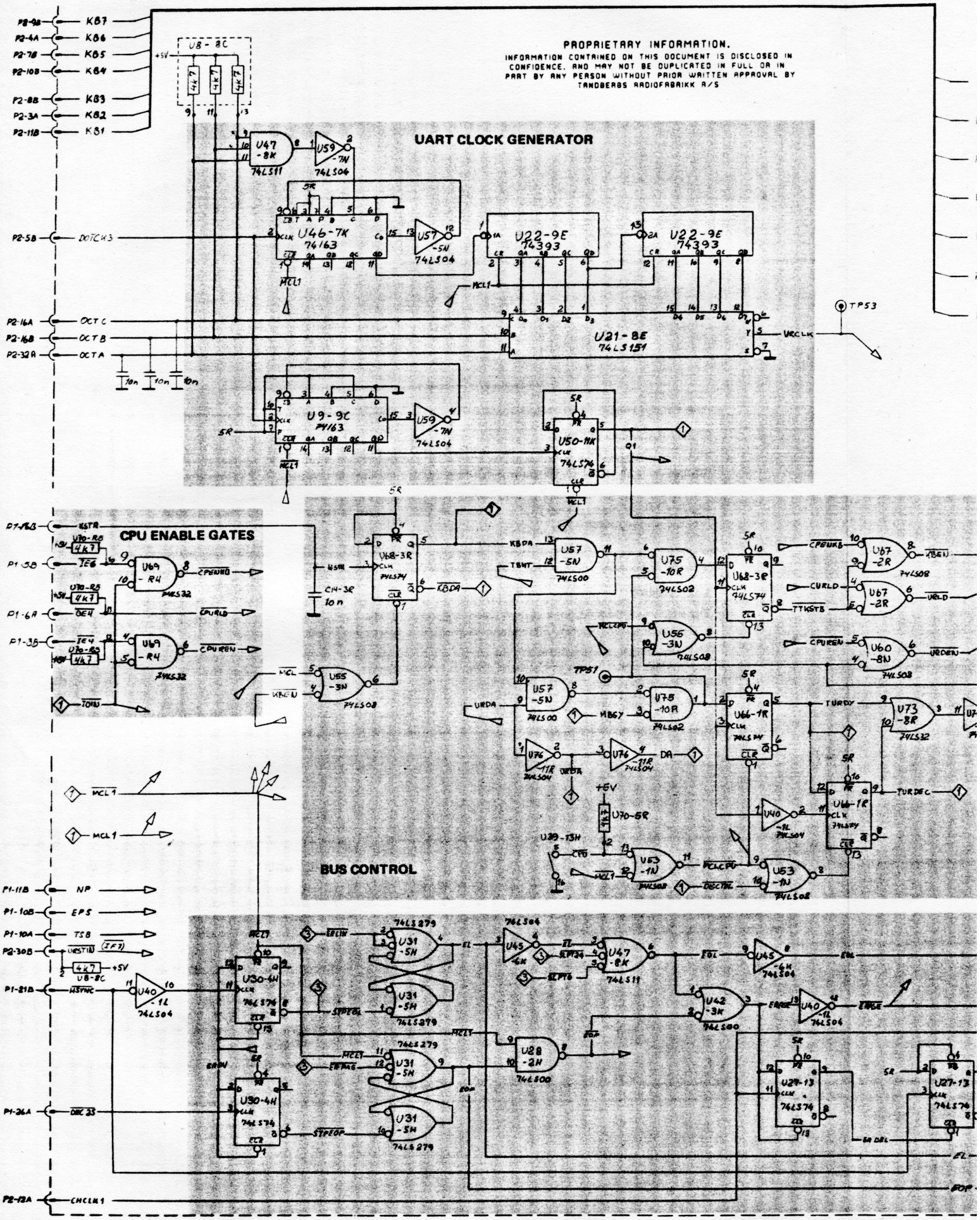
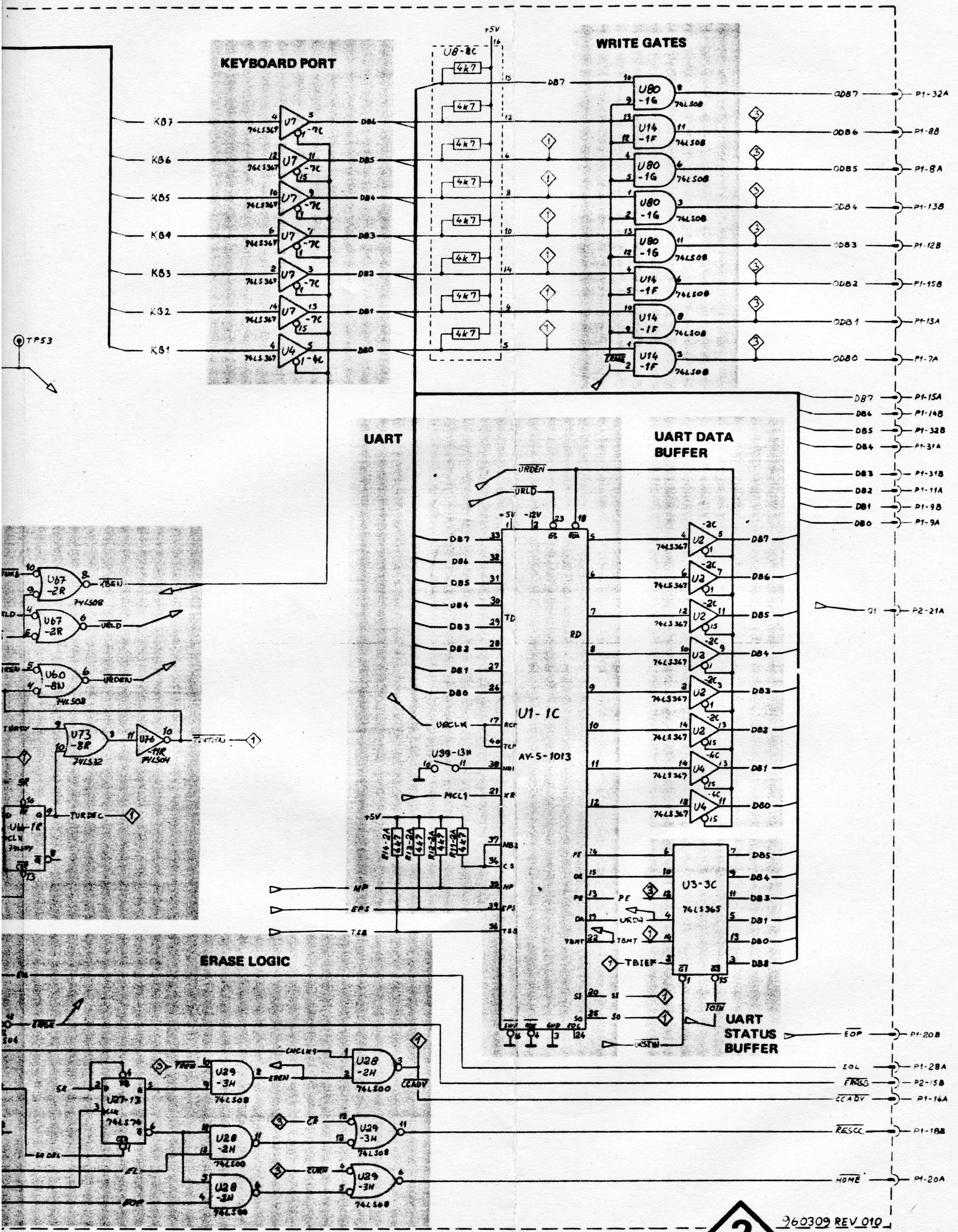


See TIMING DIAGRAM 1 page 41
and TIMING DIAGRAM 2 page 43.


KEYBOARD PORT
WRITE GATES
UART
UART DATA BUFFER
ERASE LOGIC
UART STATUS BUFFER
U8-8C
+5V
4k7
KB7
KB6
KB5
KB4
KB3
KB2
KB1
TP53
74LS367
74LS08
74LS00
74LS32
74LS04
74LS365
74LS74
U1- 1C
AY-5-1013
TD
RD
URDEN
URLD
URCLK
MCL1
U39-13H
NP
EPS
TSB
PE
URDA
TBMT
TBIEF
TOTN
EOP
EOL
ERASE
CCADV
RESCC
HOME
P1-32A
P1-8B
P1-8A
P1-13B
P1-12B
P1-15B
P1-13A
P1-7A
P1-15A
P1-14B
P1-32B
P1-31A
P1-31B
P1-11A
P1-9B
P1-9A
P2-21A
P1-20B
P1-28A
P2-15B
P1-16A
P1-18B
P1-20A
U3-3C
U73 -8R
U76 -11R
U67 -2R
U60 -8N
U28 -2H
U29 -3H
U27-13
960309 REV 010

DECODER LOGIC

Analyzes the character code present at the data bus and decides what to do with the code.
If all bits in the character code are binary 1, the character is not supposed to be written into the RAM and consequently the NONWR signal is generated inhibiting the Write Logic.

If ASCII bits 6 and 7 (ODB5 and ODB6) are both binary 0, the code belongs to a control character and will have to be decoded. Consequently TRLDEC is generated as soon as the CTRLEN goes true, also resulting in a NONWR pulse.

The decoding of control character codes takes place in the four decoders U16, U17, U18, and U19. CTRLDEC goes to the enable input G2B of all decoders. Selection of the appropriate decoder is accomplished by using data bits 3 and 4 as enabling signals for decoder inputs G1 and G2A. ODB3 selects upper or lower part of the columns whereas ODB selects column 0 or 1 in the ASCII code table.

VIDOF is true when flip-flop U43-4 is set when STX is decoded and remains true until the flip-flop is reset by ETX being decoded. SETB8 is binary 1 when UL is decoded and remain binary 1 until ND has been decoded.

ROLL LOGIC

Roll is initiated by ROLUP or RLDWN from the decoder or by ROLLF if switch U39-9 is closed and the cursor is in the bottom line. Clock pulses are then applied to the Roll Counter and the Erase Logic is initialized by SLPTO (Roll Down) or by SLPT24 (Roll Up) which also control the Line Clamp. STPEOL resets the flip-flop U31 when the erase function is completed.

ROLL COU

Holds the a
ROLUP, or
parallel out
counter cou

ROLL ADDER

Adds the output of the Roll Counter to
selected by the Address Selector. Thus th
line in the RAM can be displayed in any
although the cursor remains in the same
roll.

LAMP LOGIC

Decoding af NAK, ACK, and ENQ sets the flip-flops U25-7, 13, an so that the corresponding pilot lights come on. The lights remain c until the flip-flop is reset by the CLEAR key (CLEARK) or by CP provided the switch U39-2 is closed. If instead switch U39-1 is clos the flip-flop is reset by the SYN code being decoded.

The ERROR light comes on when U25-4 is set by PE (parity error DA at the same time from the UART. The light is reset by eithe CPCLR or CLEARK.

SPEED SENSING LOGIC

The monostable U56-5 which is set by the CCUP pulses will not return to its cleared state if it is retriggered by another CCUP pulse before the pulse time determined by C15/R18 has elapsed.

If then the time gap between consequtive CCUP pulses is shorter than the preset time interval, flip-flop U58-8 is set so that CURBL goes true. CURBL then remains true until the pulse rate falls below the preset limit.

BELL LOGIC

The ocillator U54-8 which is turned on by a pulse from the monostable U56-13 generates a 2 kHz burst approximately 70 ms long to produce a short tone in the loudspeaker.

The monostable is triggered when the cursor goes into the 72nd position (DEC72) except when the CURBL signal is true at the same time. It is furthermore always triggered when the BEL character is decoded.

ROLL COUNTER

Holds the accumulated number of rolls by counting RLDWN, ROLUP, or ROLLF being received by the Roll Logic. The parallel output of the counter is applied to the Roll Adder. The counter counts to 24 and then resets to 0.

LINE CLAMP

Ignores the line address from the Address Selector in rol tion and is instead clamped at 0 (Roll Down) or 24 (Rol the load input signals from the Roll Logic. This number as an address for the Display Ram to erase (write zeroes) 0 or line 24.

During the vertical flyback the content of text line 0 is t ferred to the Refresh Memory while the Text Line Coun busy counting to 28 and consequently cannot be used address for the RAM. Instead VBLANK and TREN to makes the Clamp present zeroes as the line number inpu Roll Adder.

ROLL ADDER

Adds the output of the Roll Counter to the text line address selected by the Address Selector. Thus the content of any text line in the RAM can be displayed in any text line on the screen although the cursor remains in the same vertical position during roll.

LAMP LOGIC

Decoding af NAK, ACK, and ENQ sets the flip-flops U25-7, 13, and 9 so that the corresponding pilot lights come on. The lights remain on until the flip-flop is reset by the CLEAR key (CLEARK) or by CPCLR provided the switch U39-2 is closed. If instead switch U39-1 is closed the flip-flop is reset by the SYN code being decoded.

The ERROR light comes on when U25-4 is set by PE (parity error) and DA at the same time from the UART. The light is reset by either CPCLR or CLEARK.

SPEED SENSING LOGIC

The monostable U56-5 which is set by the CCUP pulses will not return to its cleared state if it is retriggered by another CCUP pulse before the pulse time determined by C15/R18 has elapsed.

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The monostable is triggered when the cursor goes into the 72nd position (DEC72) except when the CURBL signal is true at the same time. It is furthermore always triggered when the BEL character is decoded.

ROLL COUNTER

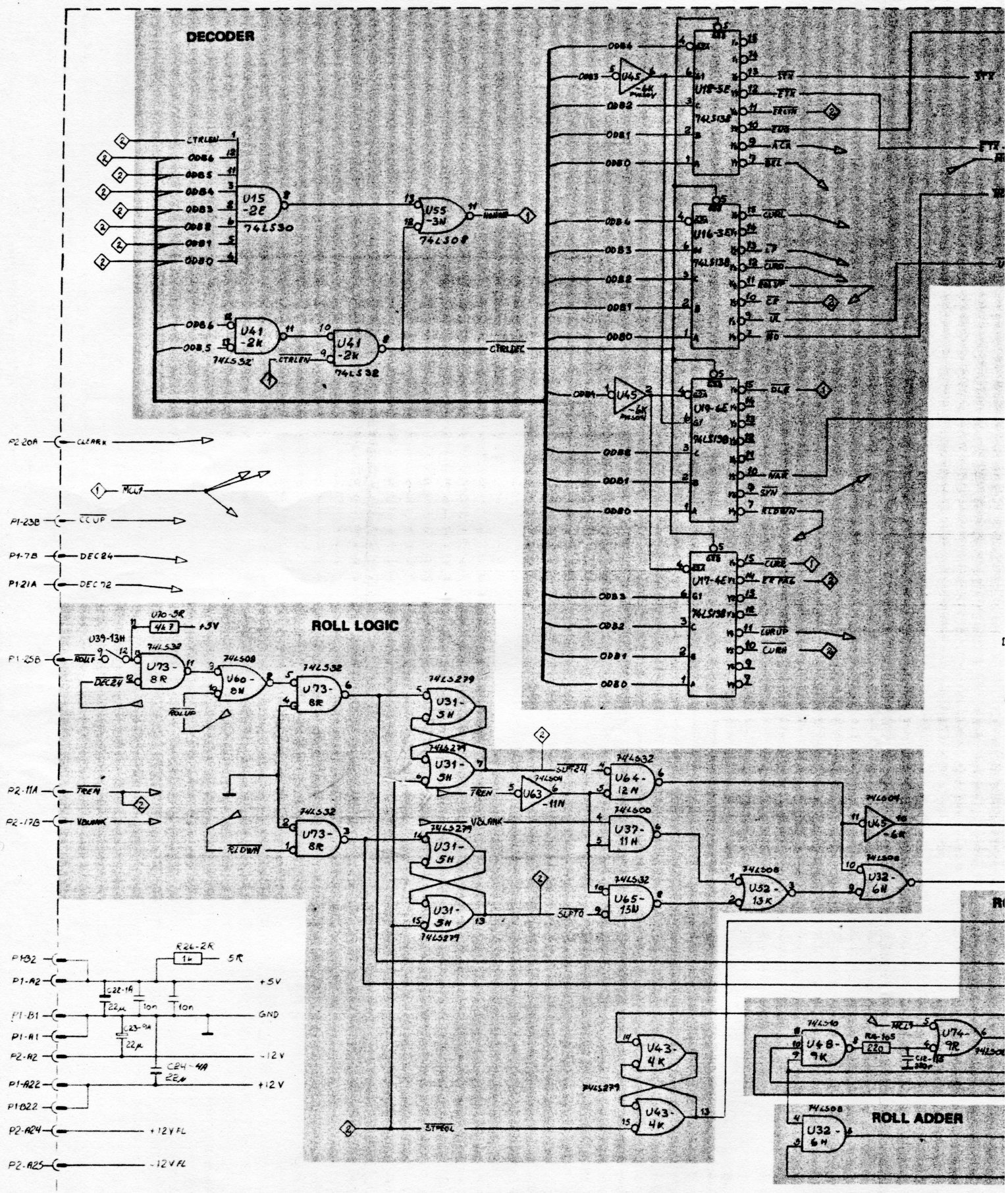
Holds the accumulated number of rolls by counting RLDWN, ROLUP, or ROLLF being received by the Roll Logic. The parallel output of the counter is applied to the Roll Adder. The counter counts to 24 and then resets to 0.

LINE CLAMP

Ignores the line address from the Address Selector in roll operation and is instead clamped at 0 (Roll Down) or 24 (Roll Up) by the load input signals from the Roll Logic. This number is used as an address for the Display Ram to erase (write zeroes) in line 0 or line 24.

During the vertical flyback the content of text line 0 is transferred to the Refresh Memory while the Text Line Counter is busy counting to 28 and consequently cannot be used as an address for the RAM. Instead VBLANK and TREN together makes the Clamp present zeroes as the line number input to the Roll Adder.

of the Roll Counter to the text line address
ddress Selector. Thus the content of any text
an be displayed in any text line on the screen
or remains in the same vertical position during



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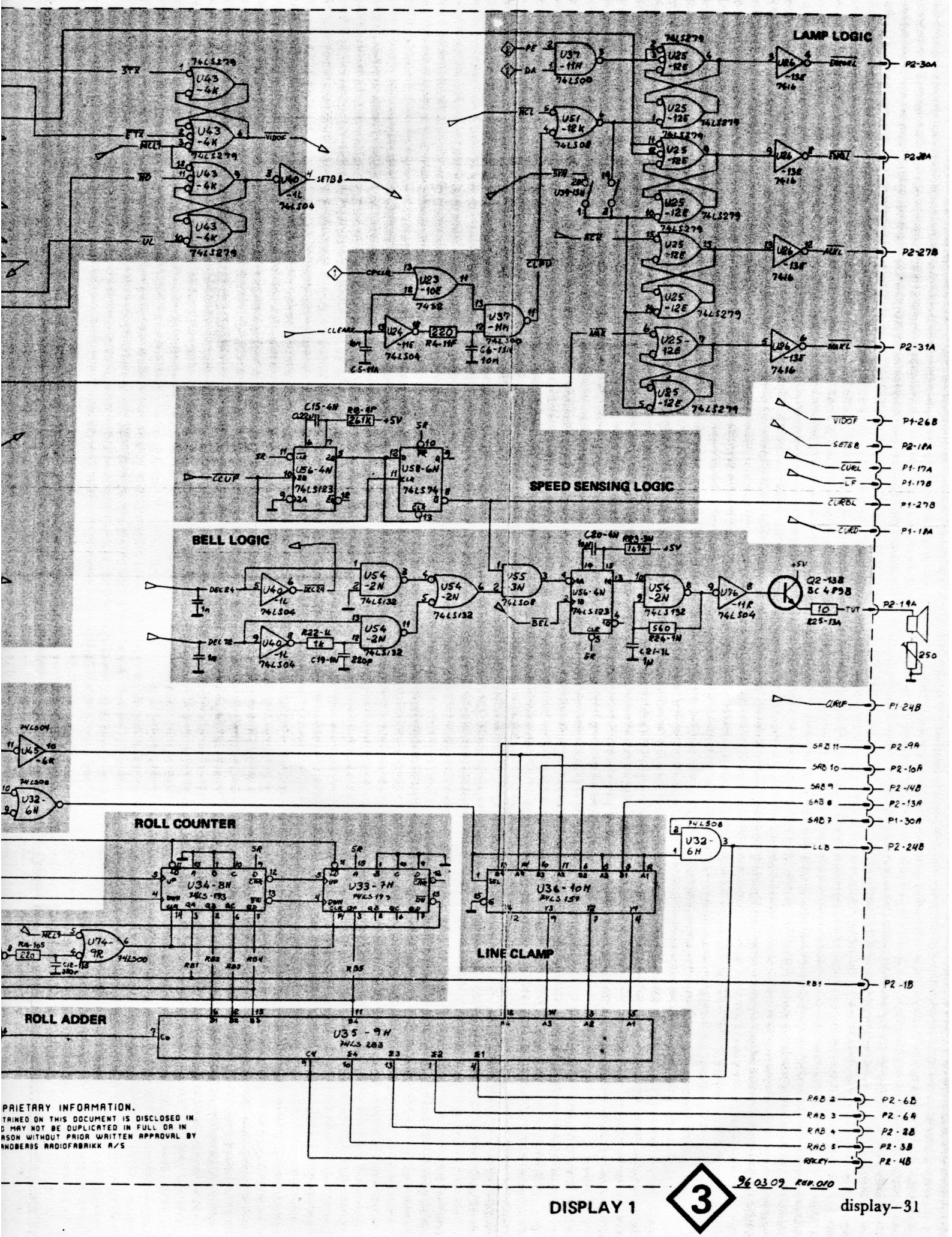


ADDRESS PROM

Contains the numbers that must be subtracted from address received via the Roll Adder in order to pack data in the Display RAM without leaving empty areas. The carry bit from the Roll Adder (RACRY) selects the PROM chip (U23 or U24. The other bits from the Roll Adder are used as address for the selected chip.

ADDRESS MODIFIER

Consists of the two adders U25 and U26. One set of inputs receive the selected address (SAB4 to 6 direct from the Address Selector and RAB1 to 4 from the Roll Adder). The other set of inputs receive the appropriate number from the Address PROM. This number consisting of APB1 to APB7 is on 2's complement form with negative sign. This means that the adder actually carries out a subtraction of the required number.

DISPLAY RAM

Consists of the sixteen 1 kbits RAMs U27 to U42 which are organized in two stachs, each stack having the capability to store 1024 8-bit words. The 8-input bits are ODB0 to ODB6 with the addition of ODB7 or SETB8. The appropriate stack is selected by MAB7 and then enabled for write-in when RAMWRP is true. Read-out from the RAM is always possible from the location defined by the address without any enabling pulse being required.

MEMORY BUSY LOGIC

The gate U47-8 ensures that the MBSY signal is always true when the RAM is in a transfer cycle (TRAFER true) or during an erase operation (ERASE true). The MBSY signal ensures that writing in is not attempted when the RAM is already busy.

iive the selected
to 4 from the
mber from the
2's complement
ies out a subtrac-

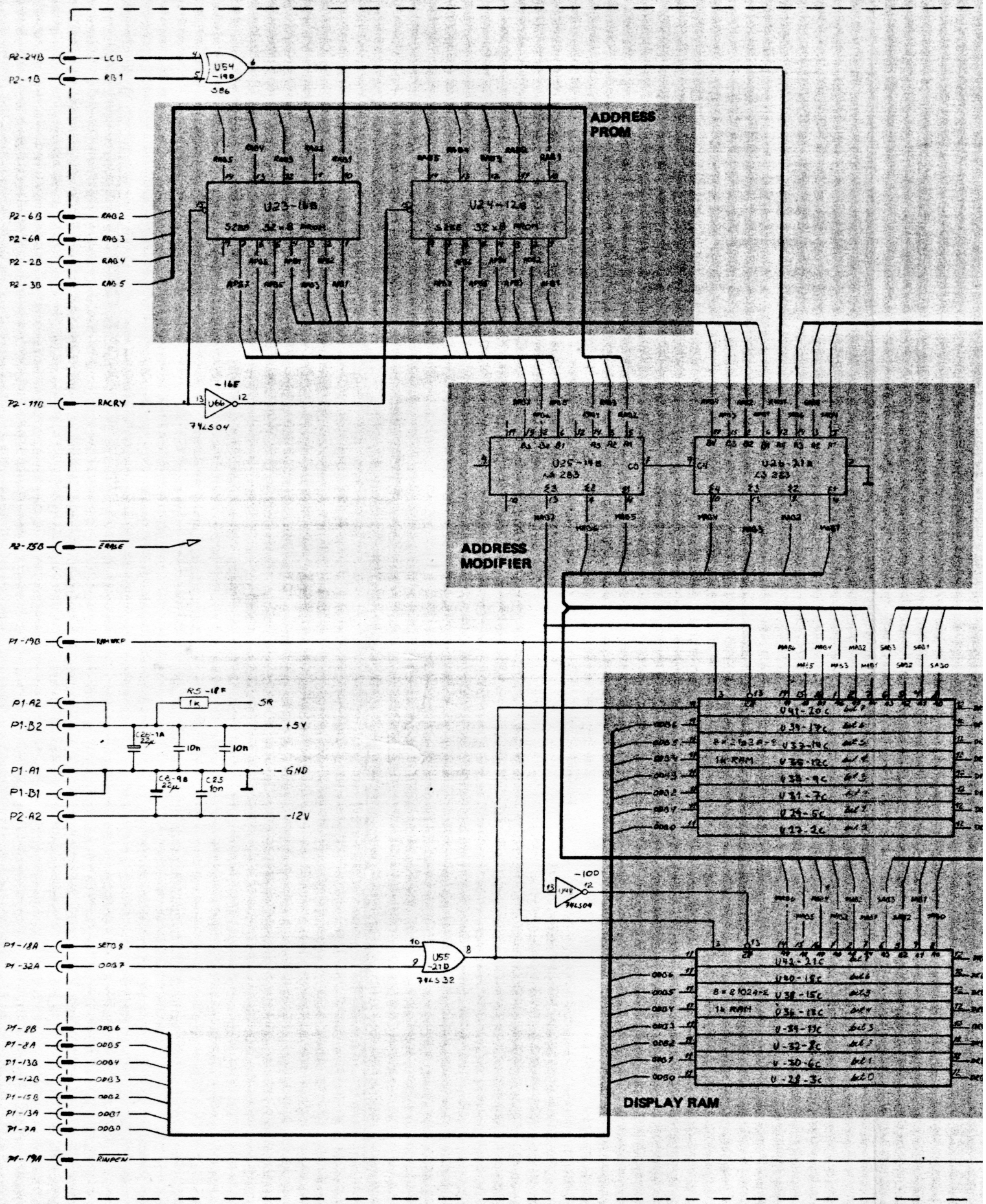
REFRESH MEMORY

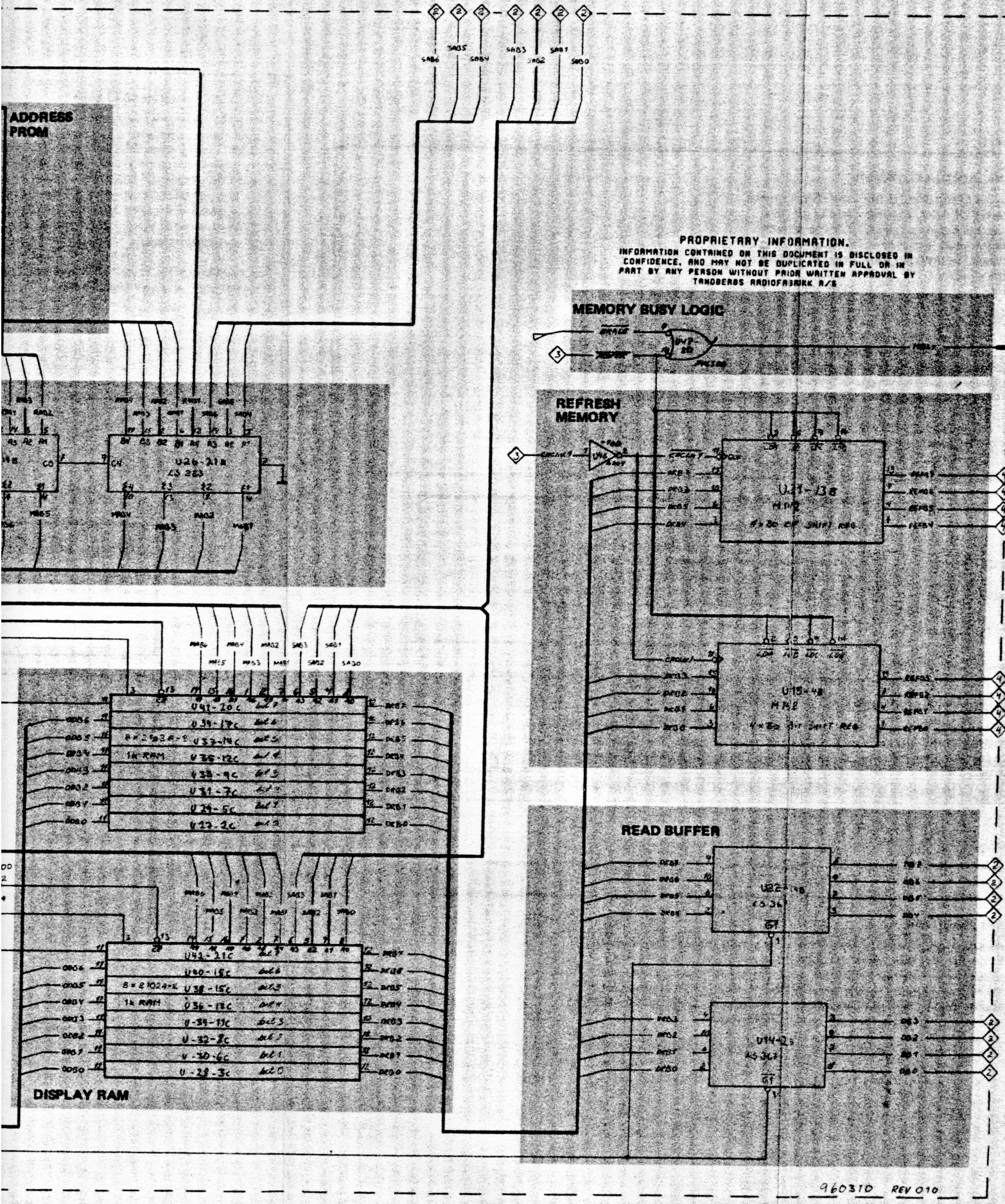
In scan 13 of every text line, TRAFER is true and enables the shift registers U15 and U29 so that data from the RAM locations addressed by the Text Line Counter (or modified by the Roll Adder) and 80 pos. upwards are clocked in by the CHCLK1 pulse train. During the next 13 scans (until TRAFER is true again) the data bits for the text line is shifted around under control of CHCLK1. Output data is available from the Refresh Memory at the shift register outputs.

U27 to U42 which are organized
capability to store 1024 8-bit
ODB6 with the addition of ODB7
elected by MAB7 and then enabled
Read-out from the RAM is always
the address without any enabling

READ BUFFER

Transfer of data from the RAM to the data bus (read-out) takes place when the RAM Input Enable (RINPEN) signal is set up by the CPU.


ADDRESS PROM
ADDRESS MODIFIER
DISPLAY RAM
P2-24B
LCB
P2-1B
RB1
U54
-19D
74S86
P2-6B
RAB2
P2-6A
RAB3
P2-2B
RAB4
P2-3B
RAB5
U23-18B
U24-12B
P2-11B
RACRY
-16F
74LS04
U25-14B
U26-21B
74S283
P2-15B
ERASE
P1-19B
RAMWRP
P1-A2
P1-B2
P1-A1
P1-B1
P2-A2
RS -18F
1K
5R
+5V
GND
-12V
C25-1A
22µ
10n
C26-9B
22µ
C25
10n
U41-20C
U39-17C
U33-14C
U38-12C
U36-9C
U31-7C
U29-5C
U27-2C
1K RAM
-10D
74LS04
P1-18A
SETDB
P1-32A
ODB7
U55
-21D
74LS32
U43-21C
U40-18C
U38-15C
U34-13C
U-34-11C
U-32-8C
U-30-6C
U-28-3C
8 x 2102A-4
P1-8B
ODB6
P1-8A
ODB5
P1-13B
ODB4
P1-12B
ODB3
P1-15B
ODB2
P1-13A
ODB1
P1-7A
ODB0
P1-19A
RWPEN



HORIZONTAL CURSOR COUNTER

Counts up on the CURAD pulse from the Write Control (Display 1) or the CCADV from the Erase Logic (Display 1), and counts down on the CURL pulse occuring when a cursor-left code is decoded. The output of the Horizontal Cursor Counter thus represents the horizontal location of the cursor.
Decoding of the counter outputs gives DEC79, DEC72, and DEC80.

The Counter is cleared when a cursor-home signal is decoded, after the 80th character position (DEC80), by RESCC which arrives from the Erase Logic at the beginning of an erase operation or when a borrow pulse occurs as a result of counting down to zero.

The Counter can be loaded with a character from the data bus if the LHC signal is true.

HORIZONTAL COMPARATOR

Compares the outputs of the Horizontal Cursor Counter and the Character Counter and generates a HCMP pulse when they agree provided the comparator is enabled (pin 3 high). If the switch U61-1/10 is open as shown, the comparator is always enabled and a block cursor will be the result. If the switch is open, the comparator is enabled only in scan 12 giving an underscore cursor.

CHARACTER COUNTER

Counts CHCLK1 pulses which occur during each text line. The output of the counter thus represents the horizontal position of the CRT beam. The Counter resets itself after count 79 and at the same time provides the CH79 signal to the Margin Counter ◈.

The counter output is used as address for the Display RAM during the refresh scan.

ADDRESS SELECTOR

When the select inputs are high (pin 1) the B inputs are selected and presented at the Y outputs. In other words the output of the Horizontal and Vertical Cursor Counters are selected in all scans except in the 13th scan of each text line (TRAFER true) in the time interval defined by POS 16-31 (during the horizontal fly-back). Then the outputs of the Character Counter and the Text Line Counter are selected as address for the Display RAM.

VERTICAL CURSOR COUNTE

Its output represents the vertical
Counts one up whenever a curso
(CURD) except when DEC24 is
incremented by the LF signal, ar
of each line. However, DEC80 is
erase line operation is carried ou
when a cursor-home code is decc
DEC25 or when a borrow pulse
counting down to zero.

The counter can be loaded with
the data bus if the LVC signal is

VERTICAL

Compares th
Counter and
true. COMP
the screen.

TEXT LINE

Counts TRA
the counter
screen, and i
The counter

VERTICAL CURSOR COUNTER

Its output represents the vertical position of the cursor. Counts one up whenever a cursor-down code is decoded (CURD) except when DEC24 is true. The counter is also incremented by the LF signal, and by DEC80 at the end of each line. However, DEC80 is stopped by EOL if an erase line operation is carried out. The counter is cleared when a cursor-home code is decoded (HOME), by the DEC25 or when a borrow pulse occurs as a result of counting down to zero.

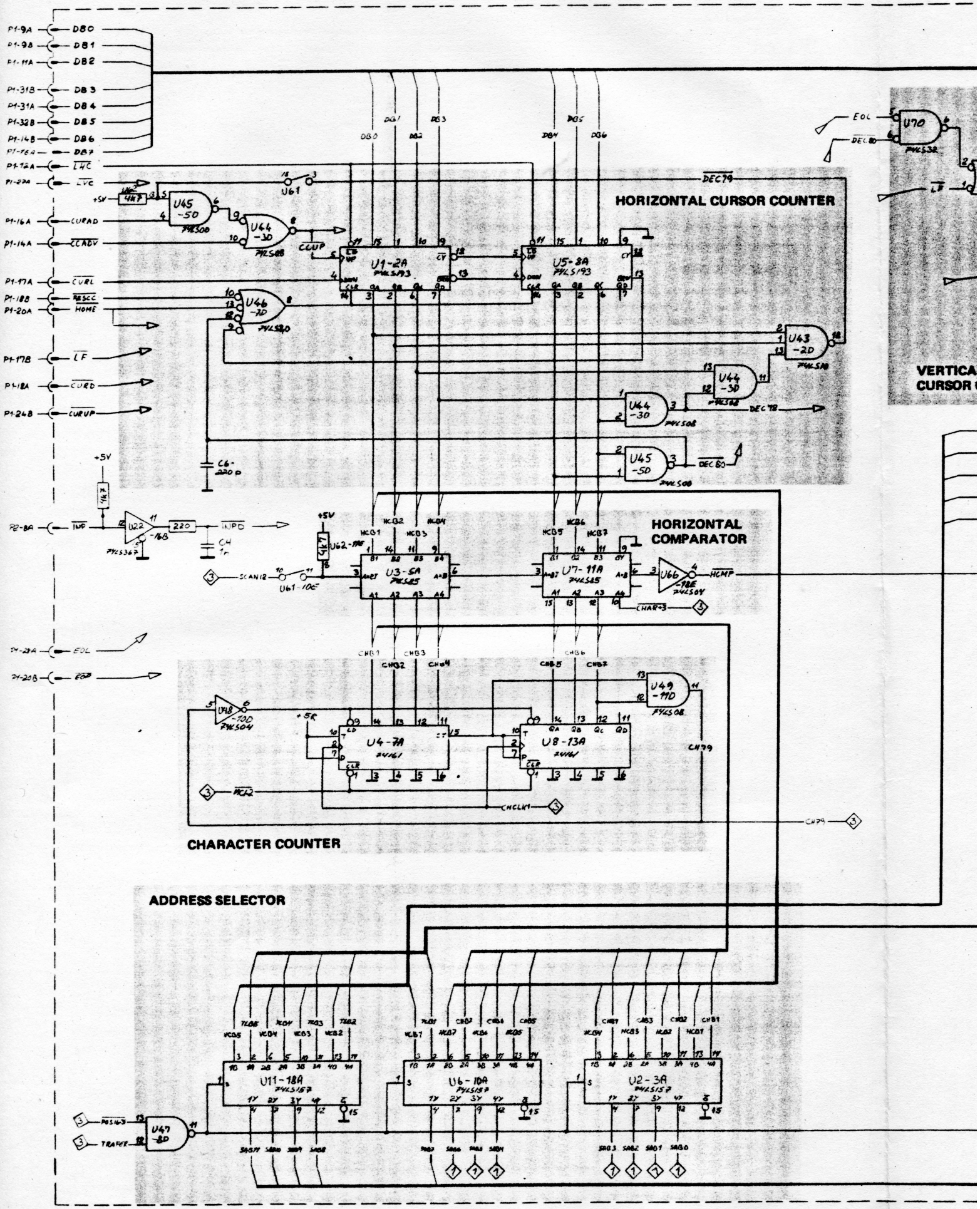
The counter can be loaded with a character code from the data bus if the LVC signal is true.

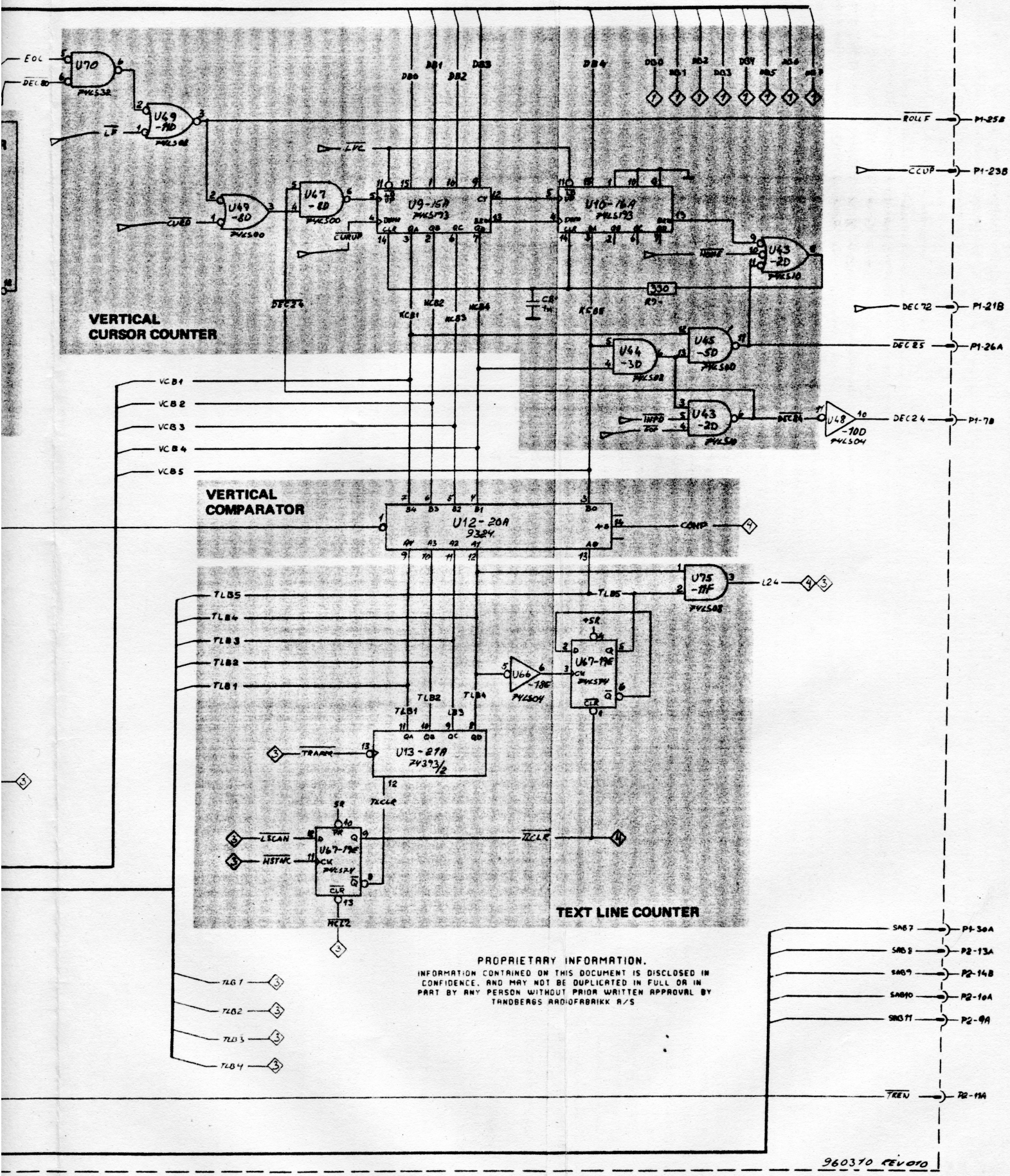
VERTICAL COMPARATOR

Compares the outputs of the Vertical Cursor Counter and the Text Line Counter and generates the COMP signal during the time interval when HCMP is true. COMP thus defines the horizontal and vertical position of the cursor on the screen.

TEXT LINE COUNTER

Counts TRAFER pulses which occur in scan 13 each text line. The output of the counter thus represents the vertical position of the CRT beam on the screen, and is used as address for the Display RAM during the refresh scan. The counter is cleared at the bottom of the page by LSCAN.


HORIZONTAL CURSOR COUNTER
HORIZONTAL COMPARATOR
CHARACTER COUNTER
ADDRESS SELECTOR
VERTICA
CURSOR
P1-9A DB0
P1-9B DB1
P1-11A DB2
P1-31B DB3
P1-31A DB4
P1-32B DB5
P1-14B DB6
P1-16A CURAD
P1-14A CCADV
P1-17A CURL
P1-18B HSCC
P1-20A HOME
P1-17B LF
P1-18A CURD
P1-24B CURUP
P2-8A INP
P1-23A EOL
P1-20B EOP
U1-2A
U5-8A
U3-5A
U7-11A
U4-7A
U8-13A
U11-18A
U6-10A
U2-3A
U45 -5D
U44 -3D
U46 -2D
U43 -2D
U47 -8D
U49 -11D
U70
U61
U62-11E
U66 -12E
U22 -16B
U48 -7D
DEC79
DEC78
DEC83
EOL
DEC80
LF
+5V
4k7
220
C6- 220 p
C4 1n
INPD
SCAN12
U61-10E
HCMP
CHAR+3
CH79
CHCLK1
POS4-3
TRAFFF
See TIMING DIAGRAM 3 page 45.


VERTICAL CURSOR COUNTER
VERTICAL COMPARATOR
TEXT LINE COUNTER
U70
U49 -9D
U49 -8D
U67 -8D
U9-15A
U10-16A
U43 -2D
U45 -5D
U44 -3D
U48 -10D
U12-20A 9324
U75 -11F
U67-9E
U66 -12E
U13-21A 74393/2
U67-9E
ROLLF
CCUP
DEC72
DEC25
DEC24
CONP
L24
TRARR
LSCAN
HSYNC
TLCLR
HCL2
TREN
SAB7
SAB8
SAB9
SAB10
SAB11
VCB1
VCB2
VCB3
VCB4
VCB5
TLB1
TLB2
TLB3
TLB4
TLB5
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960370 REV010

DOT CLOCK GENERATOR

The crystal oscillator can be stopped by strapping TP1 to ground. If desired, an external clock signal can then be applied to TP2. The main purpose of the Dot Clock signal is to shift the character dot patterns through the parallel-to-series converter (sheet 4).

SCAN COUNTER

Clocked by the HS
text line. Count 13
scan 13 which caus

DIVIDER

Divides by three to give the DOTCLK 3 signal which is used by the UART Clock Generator on Display 1 to derive the URCLK signal.

SC
Bi
is
fro
LS
has

VERTICAL TIMER

The L24 which represents text l
generate VSYNC during the TRA
is further divided in U13 to give
L24 and TLB5 gives the LLIN d
25.

CHARACTER CLOCK GENERATOR

Counts DOTCLK pulses. When the counter is full and SHRGLD goes low, the counter is loaded by 8. At the next positive transition of DOTCLK counting starts from 8. SHRGLD thus occurs once every 9 DOTCLK pulses.

CLOCK GATE

Allows the CHCLK to pass as the CHCLK 1 signal to the Margin Counter during the CHAR signal and the CH80 pulse.

MARGIN COUNTER

Each horizontal scan lasts for 111 cycles of the CHCLK signal corresponding to 49.25 us. The timing of the various events during the scan is controlled by the Margin Counter which starts to count CHCLK pulses at the end of the horizontal blanking pulse. The binary-to-decimal decoder U56 makes the CHAR signal true at the transition to count 4 and thus allows the CHCLK signal to pass through the Clock Gate. At the same time the COUNT signal goes false and stops the Margin Counter.

The gated Clock signal CHCLK1 now clocks the Character Counter 2 while the CRT beam moves from the 1st to the 80th character position on the screen: At count 79 this counter generates the CH79 pulse and thus clears itself. CH79 at U70-1 allows U57 to continue from 4 to 5 but since CH79 is also applied to the flip-flop U58-12 which generates the CH80 signal during the next clock period, the counter will hold the count at 5 during this clock period owing to the presence of CH80 at U57-10. The CHAR signal which disappears as soon as the Margin Counter goes from 4 to 5, stops the CHCLK1 signal and thus prevents further counting by the character counter. The Margin Counter then continues up to 31, resets to zero and starts a new cycle.

The 5th bit of the Margin Counter is implemented by the flip-flop U58. During the first 8 counts (0 to 7) U58 is in its cleared state with the Q output low. At count 8 the D output of U57 changes to high and makes the POS 8-31 signal from U71-1 go true. At the same time HSYNC starts. At count 16 the carry output of U57 goes high and clocks flip-flop U58-3 so that POS 16-31 goes true. The U57 counter starts again from 0 but this time the decoder U56 is disabled by POS 8-31.

SCAN COUNTER

Clocked by the HSYNC pulses, U63 counts scans during each text line. Count 13 is decoded to give the TRAFER signal in scan 13 which causes the counter to be loaded by 0.

SCAN DECODER

Bits 2 and 3 from the Scan Counter gives the SCAN 12 signal when TRAFER is false. Count 13 is decoded to give TRAFER in scan 13. The LLIN signal from Vertical Timer is combined with Scan Counter bits 0 and 3 to give LSCAN which clears the Text Line Counter after the last scan in text line 25 has been completed.

VERTICAL TIMER

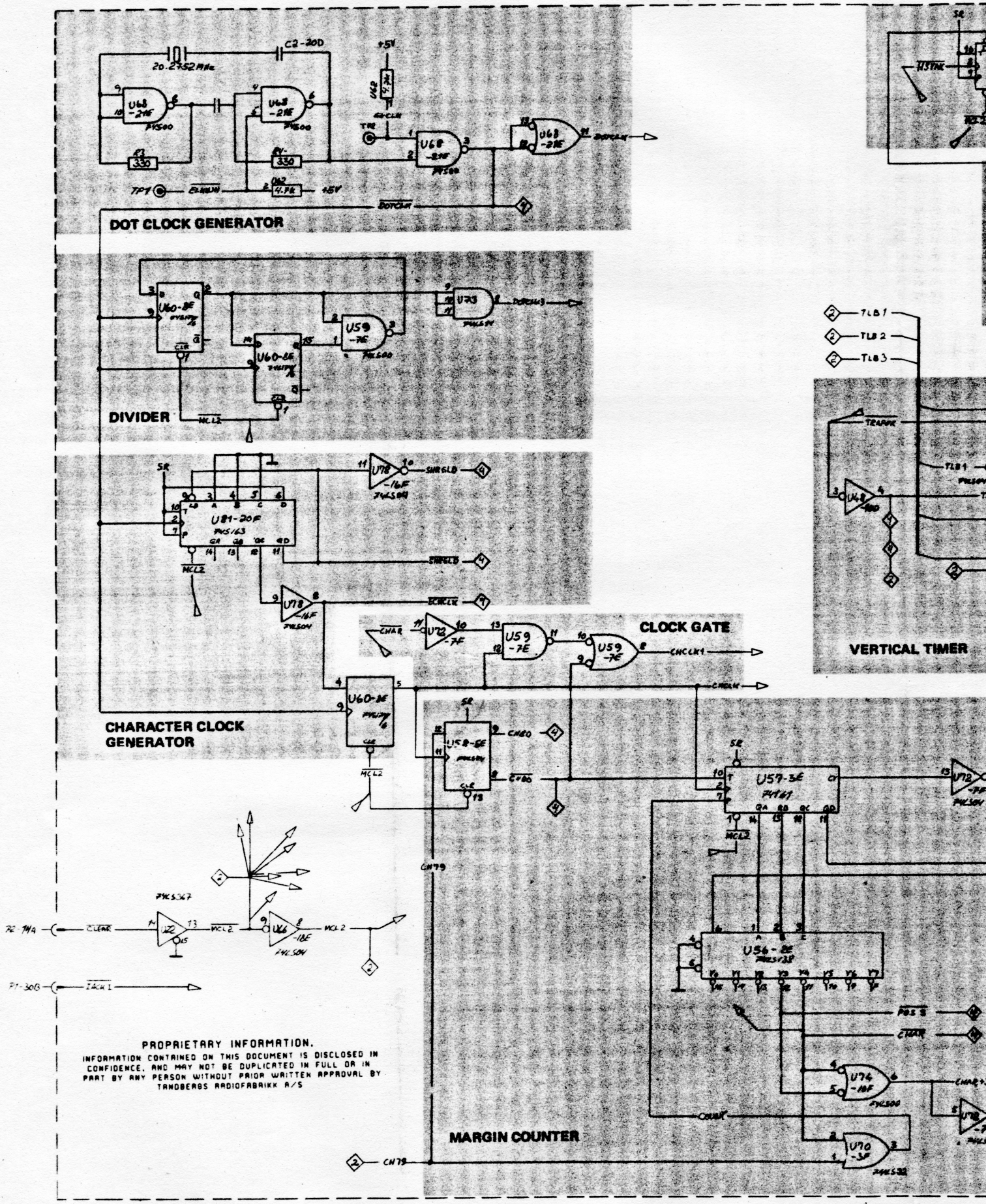
The L24 which represents text line 24 is combined with TLB1 and TLB2 to generate VSYNC during the TRAFER signal at the end of text line 25. VSYNC is further divided in U13 to give the blink frequency (BLFRQ).
L24 and TLB5 gives the LLIN during TRAFER after the last scan in text line 25.

ıck signal CHCLK1 now clocks the
ınter ◇ while the CRT beam
he 1st to the 80th character posi-
creen: At count 79 this counter
CH79 pulse and thus clears itself.
·1 allows U57 to continue from 4
CH79 is also applied to the flip-
which generates the CH80 signal
rt clock period, the counter will
ıt at 5 during this clock period
resence of CH80 at U57-10. The
which disappears as soon as the
ır goes from 4 to 5, stops the
al and thus prevents further
ıe character counter. The Margin
ontinues up to 31, resets to zero
w cycle.

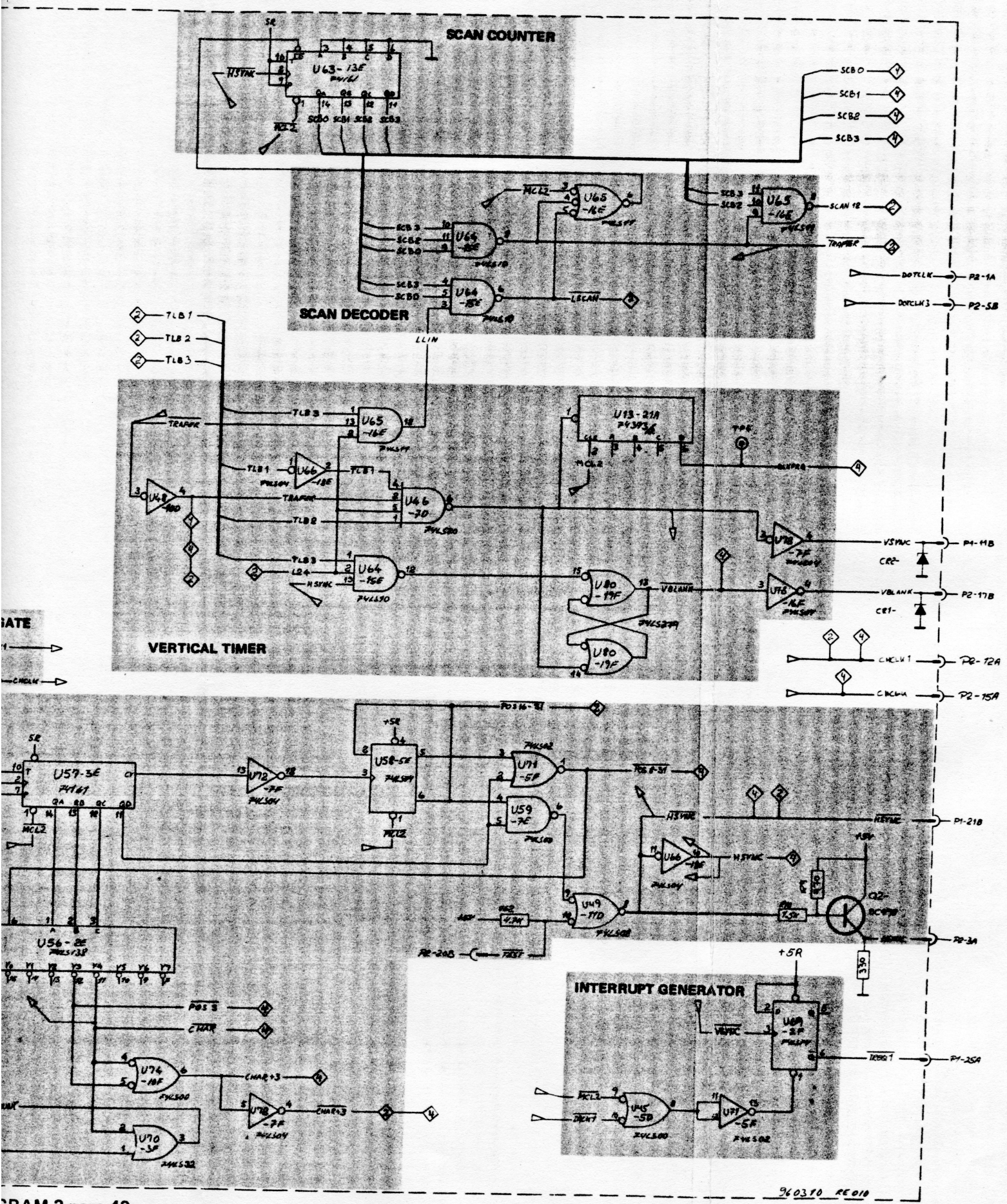
the Margin Counter is imple-
flip-flop U58. During the first 8
U58 is in its cleared state with
ow. At count 8 the D output of
high and makes the POS 8-31
1-1 go true. At the same time
At count 16 the carry output of
and clocks flip-flop U58-3 so
goes true. The U57 counter
m 0 but this time the decoder
by POS 8-31.

INTERRUPT GENERATOR

Each time VSYNC occurs the interrupt request IREQ3 will be sent to the Local CPU and will remain on until the CPU replies with IACK1.



See TIMING DIAGRAM 2 page 43, TIMING DIAGRAMs 3 and 4 page 45 and TIMING DIAGRAM 5 page 47.



GRAM 2 page 43,
Ms 3 and 4 page
IAGRAM 5 page 47.

DISPL

DOT PATTERN PROM

Contains the dot patterns for all the display characters. The patterns are stored as 8-bit words, one word for each horizontal row in the character dot matrix. Access to each word is accomplished by an 11-bit address in two parts. One part which we may call the character address consisting of REFB0 to REFB7 from the Refresh Memory points at the first row in the character matrix. The other part, the row address, consisting of 4 bits from the scan counter points at the particular row.

During one text line the character addresses which circulate in the Refresh Memory are applied to the PROM in the same sequence in all the 14 scans needed to write one particular text line. The row address is incremented by one at the beginning of each scan and goes from 0 to 13 in each text line.

BLINK LOGI

The BLFRQ w
U55-11 only
applied to the
However, the
from blinking

CURSOR LOGIC

The CURSOR signal is present when the flip-flop is in the se
with CHCLK when the COMP signal from the comparator is
horizontal and vertical cursor counters coincide with the Ch
Line Counter respectively. If the cursor switch is set for u
appears only in scan 12. When the switch is set for block cu
scans. The CURBL signal from the speed sensing Logic will
the cursor. The switches 5-16 and 6-15 determines whether
rupted at the blink frequency or whether it is steady.

PARALLEL-TO-SERIES CONVERTER

The dot pattern words from the Dot Pattern PROM are
SHRGLD is low in the intervals between the characters.
pattern word is shifted to the right at the DOTCLK rate
output, pin 13. If a clear signal is applied at pin 9 the co
quently nothing will appear on the screen. When the swi
serial input is connected to ground, and dot no. 9 will b
are changed over, GENB1 which corresponds to dot 8 is
then be the same as dot 8.

CHARACTER BLANKING CONTROL

The CONCLR signal which causes temporary blanking of the display occurs when th
INVISA signal from the Attribute Decoder is true. CONCLR is also true when flip-flo
U76 is in the cleared state. This will occur whenever ADVEN is not true and when th
left and right margins signal (CHAR+3) is false. Depending on the setting of the switc
7-14 and 9-12, the flip-flop is also cleared in the middle of a text line if an attribute
character is detected (REFB7=1) or if a control character is detected (REFB5 and
REFB6 both binary 0).

UNDERLINE MODE SELECTOR

The UMSEL signal has two differe
Attribute/Underline switch is in th
the UMSEL signal when true will
under the character. When the sw
position, the UMSEL signal when t
attribute decoder. The UMSEL si
REFB7=1 (inside left and right ma

ATTRIBUTE MEMORY

Is updated with the attribute character from the Attribute Latch in the 80th character position, scan 13 when TRAFER, CH80 and SHRGLD are all true.

ATTRIBUTE LATCH

REFB 4, 5, and 6 from the Refresh Memory are clocked into the latch if ATSEL is low. If ATSEL is high, the attribute bits stored in the Attribute Memory are clocked by the Attribute clock, ATCLK.

ATTRIBUTE CLOCK GENERATOR

The Attribute Clock pulses ATCLK will occur in Sync with the positive transitions of CHCLK when REFB7 is binary 1. They will also occur regardless of REFB7 in the character clock period before the text line (POS 3 true). In both cases the ATCLK pulse ends when ECHCLK goes low.

ATTRIBUTE SELECTOR

The ATSEL signal determines whether the Attribute latch is to be updated from the Refresh Memory or from the Attribute Memory. ATSEL is always low from the first coincidence of ECHCLK=CHAR=0 to the trailing edge of HSYNC. ATSEL goe
high at the positive transition of HSYNC if REFB7 is binary 0.
(The first character of the coming text line is then not an attribute character and hence the Attribute Latch shall be updated with the attribute from the last position of the preceding line .)

dis

BLINK LOGIC

The BLFRQ which is an alternating signal at 3.125 Hz is always present but is le
U55-11 only when the blink attribute signal BLINKA is true. The BLINKM s
applied to the Inversion Logic where it interrupts the video signal at the blink
However, the CURSOR signal being applied to U55-5 inhibits the gate and preve
from blinking when the cursor (block cursor only) shall be superimposed on the

CURSOR LOGIC

The CURSOR signal is present when the flip-flop is in the set state. This occurs in sync with CHCLK when the COMP signal from the comparator is true which means that the horizontal and vertical cursor counters coincide with the Character Counter and Text Line Counter respectively. If the cursor switch is set for underscore cursor, COMP appears only in scan 12. When the switch is set for block cursor, COMP will occur in all scans. The CURBL signal from the speed sensing Logic will clear the flip-flop and blank the cursor. The switches 5-16 and 6-15 determines whether the CURSOR signal is interrupted at the blink frequency or whether it is steady.

INVERSION C

The dot signal f
"ones" for the c
For normal vide
the inversion co
ting). This requi
signal and INVE
U54-11. With BI
back to positive
shown) the third
SOR pulse U54-
the video signal,
If it is an unders
present and cons
block cursor the
consequently the
an alternating sig
the video signal i
video. UNDLM c
it is applied to t
give a constant "
is set for normal
signal comes out
S1 is closed, ther
for any signal an
be inverted.

PARALLEL-TO-SERIES CONVERTER

The dot pattern words from the Dot Pattern PROM are parallel loaded into this converter when SHRGLD is low in the intervals between the characters. When SHRGLD goes high, the dot pattern word is shifted to the right at the DOTCLK rate and appears bit by bit at the serial output, pin 13. If a clear signal is applied at pin 9 the content of all cells will be 0 and consequently nothing will appear on the screen. When the switches 1 and 2 are set as shown, the serial input is connected to ground, and dot no. 9 will be blank (normal space). If both switches are changed over, GENB1 which corresponds to dot 8 is applied to the serial input. Dot 9 will then be the same as dot 8.

CHARACTER BLANKING CONTROL

The CONCLR signal which causes temporary blanking of the display occurs when the INVISA signal from the Attribute Decoder is true. CONCLR is also true when flip-flop U76 is in the cleared state. This will occur whenever ADVEN is not true and when the left and right margins signal (CHAR+3) is false. Depending on the setting of the switches 7-14 and 9-12, the flip-flop is also cleared in the middle of a text line if an attribute character is detected (REFB7=1) or if a control character is detected (REFB5 and REFB6 both binary 0).

BLAN

Applie
to the
tical b
the ho

UNDERLINE MODE SELECTOR

The UMSEL signal has two different tasks. When the Attribute/Underline switch is in the underline position, the UMSEL signal when true will make an underline under the character. When the switch is in attribute position, the UMSEL signal when true, will disable the attribute decoder. The UMSEL signal is true when REFB7=1 (inside left and right margins).

ATTRIBUTE MEMORY

Is updated with the attribute character from the Attribute Latch in the 80th character position, scan 13 when TRAFER, CH80 and SHRGLD are all true.

UNDERLINE

Generates the
If the underli
attribute chara
until the next
the page. If th
tion as shown
characters in w

ATTRIBUTE LATCH

REFB 4, 5, and 6 from the Refresh Memory are clocked into the latch if ATSEL is low. If ATSEL is high, the attribute bits stored in the Attribute Memory are clocked by the Attribute clock, ATCLK.

ATTRIBUTE DECODER

Presents a "low" at the output that corresponds with the binary value of attribute bits A, B, and C but only when the enable inputs G2A and G2B are low and G1 high. G2A is controlled by the Underline/Attribute switch.

UNDERLINE/

Disables the D
line position.
from the top
UMSEL disabl
also during the
is being loaded

K GENERATOR

pulses ATCLK will occur
itive transitions of CHCLK
ry 1. They will also occur
7 in the character clock
xt line (POS 3 true). In
.K pulse ends when

VERTICAL ENABLER

ADVEN goes true and enables the Attribute Decoder when TLCLR goes true and sets the flip-flop. The flip-flop is reset by VIDOF or by the combination of TLB1, L24 and HSYNC being true.

ATTRIBUTE SELECTOR

The ATSEL signal determines whether the Attribute latch is to be updated from the Refresh Memory or from the Attribute Memory. ATSEL is always low from the first coincidence of ECHCLK=CHAR=0 to the trailing edge of HSYNC. ATSEL goes high at the positive transition of HSYNC if REFB7 is binary 0. (The first character of the coming text line is then not an attribute character and hence the Attribute Latch shall be updated with the attribute from the last position of the preceding line .)

BLINK LOGIC

The BLFRQ which is an alternating signal at 3.125 Hz is always present but is let through U55-U55-11 only when the blink attribute signal BLINKA is true. The BLINKM signal is then applied to the Inversion Logic where it interrupts the video signal at the blink frequency. However, the CURSOR signal being applied to U55-5 inhibits the gate and prevents the text from blinking when the cursor (block cursor only) shall be superimposed on the text.

when the flip-flop is in the set state. This occurs in sync
ignal from the comparator is true which means that the
ounters coincide with the Character Counter and Text
he cursor switch is set for underscore cursor, COMP
he switch is set for block cursor, COMP will occur in all
the speed sensing Logic will clear the flip-flop and blank
nd 6-15 determines whether the CURSOR signal is inter-
r whether it is steady.

ONVERTER

the Dot Pattern PROM are parallel loaded into this converter when
vals between the characters. When SHRGLD goes high, the dot
e right at the DOTCLK rate and appears bit by bit at the serial
nal is applied at pin 9 the content of all cells will be 0 and conse-
on the screen. When the switches 1 and 2 are set as shown, the
ground, and dot no. 9 will be blank (normal space). If both switches
hich corresponds to dot 8 is applied to the serial input. Dot 9 will

the display occurs when the
CLR is also true when flip-flop
VEN is not true and when the
g on the setting of the switches
of a text line if an attribute
er is detected (REFB5 and

RLINE MODE SELECTOR

MSEL signal has two different tasks. When the
ute/Underline switch is in the underline position,
MSEL signal when true will make an underline
the character. When the switch is in attribute
n, the UMSEL signal when true, will disable the
te decoder. The UMSEL signal is true when
7=1 (inside left and right margins).

TE LATCH

, and 6 from the Re-
ory are clocked into
f ATSEL is low. If
high, the attribute
in the Attribute Me-
locked by the Attri-
, ATCLK.

INVERSION CONTROL

The dot signal from the parallel-to-series converter is always positive Logic, with "ones" for the dots in the character pattern and "zeroes" for the background. For normal video with white characters on a black screen the dot signal out of the inversion control must be in negative Logic (because video gate also is inverting). This requires an odd number of inversions. In the absence of a CURSOR signal and INVERA false, U54-3 is high and causes one inversion to take place at U54-11. With BLINKM and UNDLM also false the dot signal appears inverted back to positive logic at U53-8. If finally switch S1 is set for normal video (as shown) the third and required inversion takes place at U54-8. During the CURSOR pulse U54-3 changes to low. Considering this negative logic CURSOR as the video signal, only two inversions are required in normal video display mode. If it is an underscore cursor, the dot signal is always zero when the cursor is present and consequently no inversion takes place at U54-11. In the case of a block cursor the dot signal is not inverted at U54-11 because U54-12 is low and consequently the character comes out black on a white block cursor. BLINKM is an alternating signal applied to the preset input U53-10 and will hence interrupt the video signal in normal as well as in inverse video. UNDLM can only occur in scan 12. Since it is applied to the clear input U53-13 it will give a constant "one" at U53-8. If the switch S1 is set for normal video as shown, the underline signal comes out in negative logic at U54-8. If S1 is closed, there will be no inversion at U54-8 for any signal and everything on the screen will be inverted.

VIDEO GATE

Lets the video signal through to the Video Board when BLANKN is true.

BLANKING GATE

Applies a blanking signal (high) to the video gate during the vertical blanking pulse and during the horizontal flyback (POS8-31).

UNDERLINE LOGIC

Generates the UNDLM signal in scan 13 (TRAFER true). If the underline mode is established by an underline attribute character (UNDLA true), UNDLM will last until the next attribute character or to the bottom of the page. If the switch U61-4,17 is in the underline position as shown, underline mode will be selected for characters in which REFB7 is binary 1.

ATTRIBUTE DECODER

Presents a "low" at the output that corresponds with the binary value of attribute bits A, B, and C but only when the enable inputs G2A and G2B are low and G1 high. G2A is controlled by the Underline/Attribute switch.

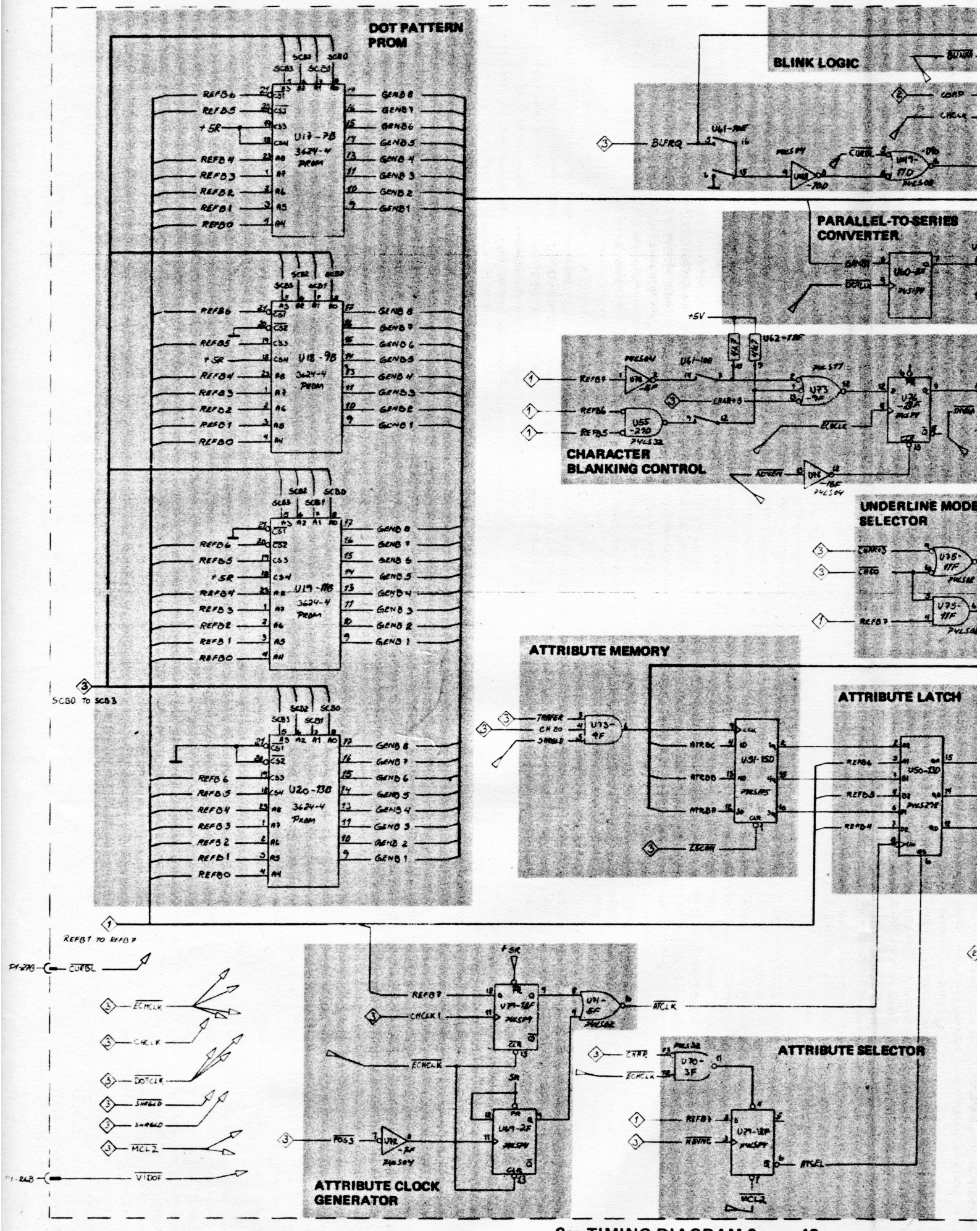
UNDERLINE/ATTRIBUTE SWITCH

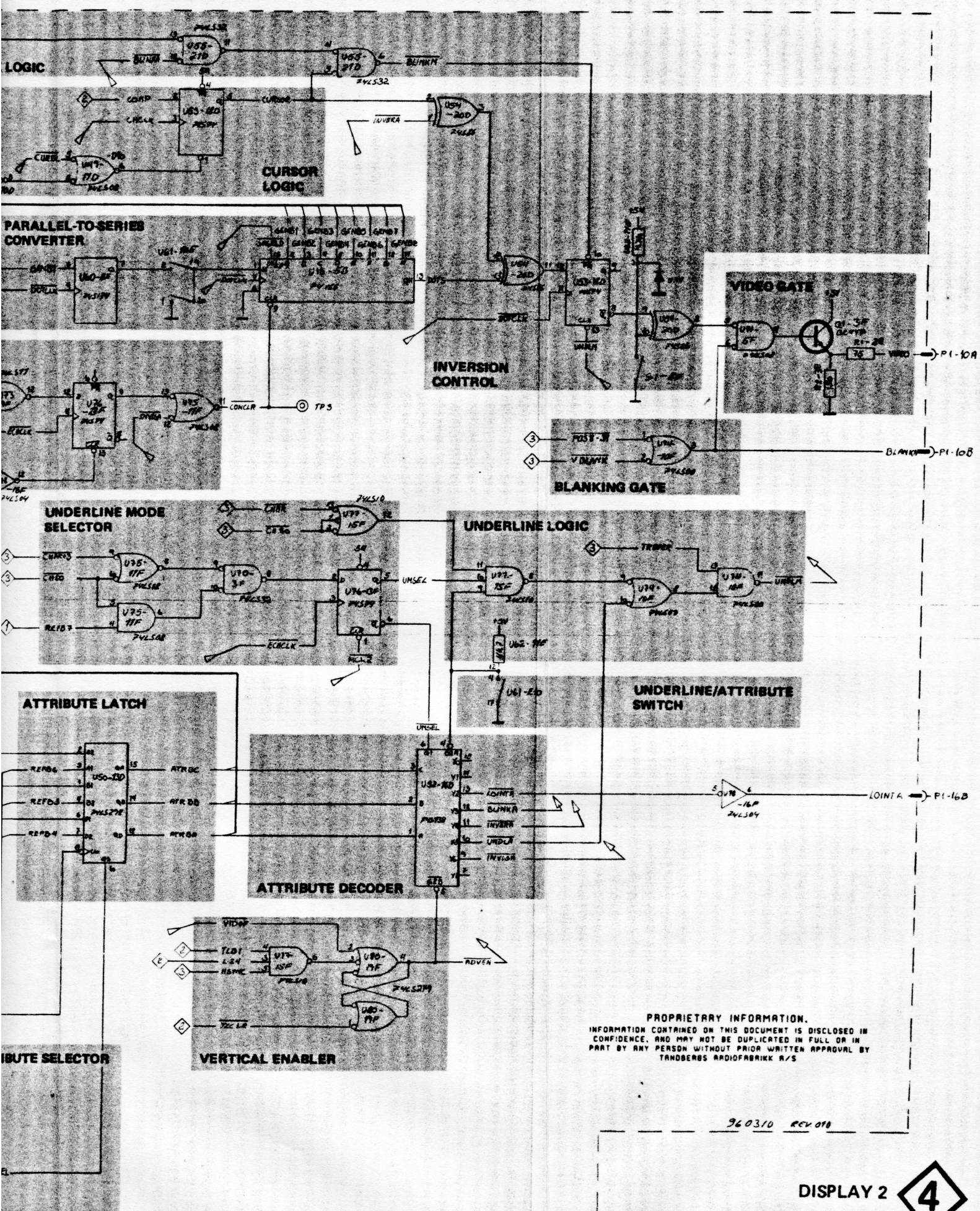
Disables the Decoder when the switch is in the Underline position. Otherwise ADVEN enables the Decoder from the top to the bottom of the display area, and UMSEL disables the Decoder outside the text line and also during the text line while a new attribute character is being loaded into the Attribute Latch.

VERTICAL ENABLER

ADVEN goes true and enables the Attribute Decoder when TLCLR goes true and sets the flip-flop. The flip-flop is reset by VIDOF or by the combination of TLB1, L24 and HSYNC being true.

ter the Attribute latch is to
ory or from the Attribute
n the first coincidence of
dge of HSYNC. ATSEL goes
YNC if REFB7 is binary 0.
ext line is then not an attri-
ute Latch shall be updated
tion of the preceding line .)


DOT PATTERN PROM
U17-7B
U18-9B
U19-11B
U20-13B
3624-4 PROM
BLINK LOGIC
PARALLEL-TO-SERIES CONVERTER
CHARACTER BLANKING CONTROL
UNDERLINE MODE SELECTOR
ATTRIBUTE MEMORY
ATTRIBUTE LATCH
ATTRIBUTE SELECTOR
ATTRIBUTE CLOCK GENERATOR
SCB0 TO SCB3
REFB1 TO REFB7
CURBL
ECHCLK
CHCLK
DOTCLK
SHFCLD
SHFCLD
MCL2
VIDOF
ATCLK
ATSEL
See TIMING DIAGRAM 2 page 43
and TIMING DIAGRAM 5 page 47.


LOGIC
CURSOR LOGIC
PARALLEL-TO-SERIES CONVERTER
INVERSION CONTROL
VIDEO GATE
BLANKING GATE
UNDERLINE MODE SELECTOR
UNDERLINE LOGIC
UNDERLINE/ATTRIBUTE SWITCH
ATTRIBUTE LATCH
ATTRIBUTE DECODER
VERTICAL ENABLER
IBUTE SELECTOR
CONCLR
TP3
VIDEO
P1-10A
BLANKM
P1-10B
LOINTA
P1-16B
UMSEL
ADVEN
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DISPLAY 2
4